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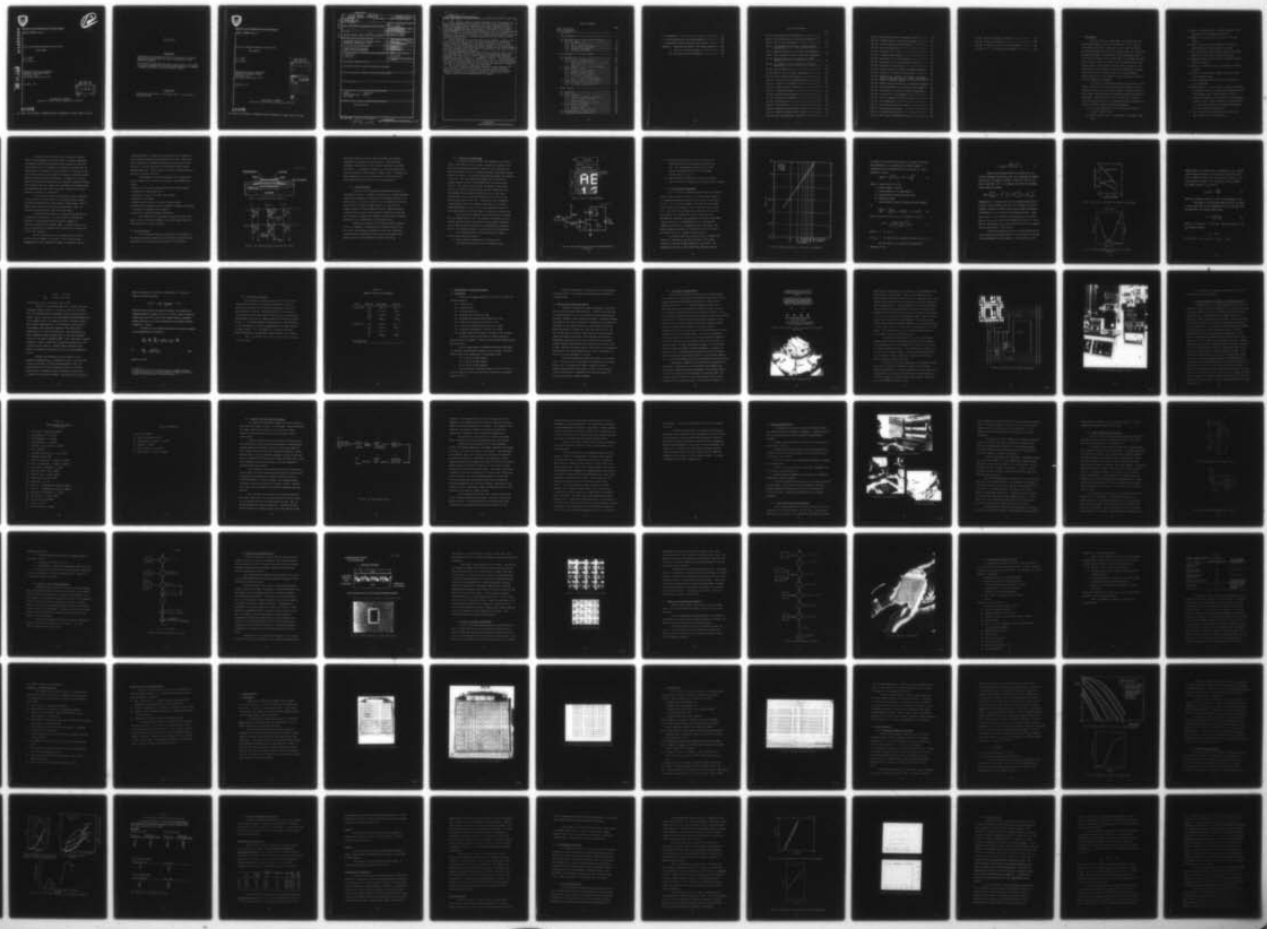

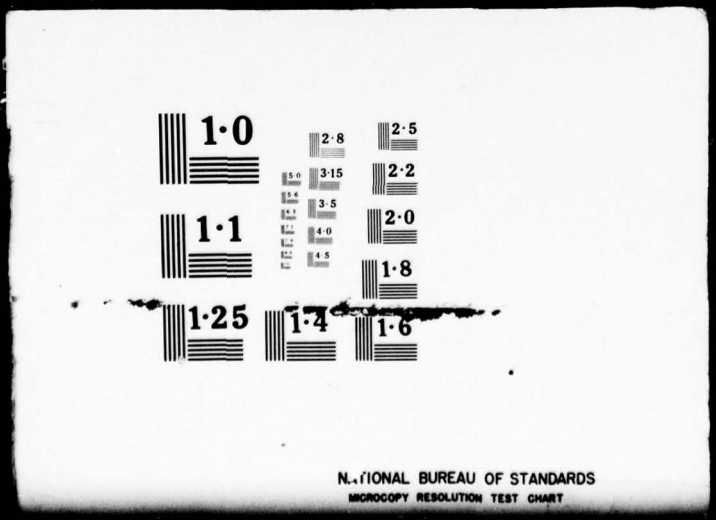

Research and Development Technical Report

Report ECOM-72-0061-12

THIN FILM TRANSISTOR-ADDRESSED DISPLAY DEVICE

FINAL REPORT

T. P. Brody
F. C. Luo
D. H. Davies

WESTINGHOUSE ELECTRIC CORPORATION
RESEARCH & DEVELOPMENT CENTER
1310 Beulah Road
Pittsburgh, Pennsylvania, 15235

September, 1977

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US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

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This is the final report on Contract DAAB07-72-C-0061; the objective of which was an examination of the feasibility of fabricating a multielement dot-matrix display using electroluminescent output and an integrated thin film transistor addressing array. The concepts have been validated, good quality functional displays were made and delivered to the US Army. Three formats were examined: 6" x 6", 20 lpi [12,000 elements], 6" x 6", 30 lpi [25,000 elements] and 6" x 3" 30 lpi [17,000 elements]; the latter display was designed to be integrated into a US Army field system, the TACFIRE forward observer terminal, and the Digital Message Device. Specimen displays are now being fitted into that device for field trials.

The TFT arrays met all the expectations of this program. Devices in the array could switch 300 V_{pp} power, they demonstrated excellent uniformities which allowed the presentation of good grey scale imagery as well as alpha-numerics. Devices with extremely low leakage currents (< 1 nA) were achieved. Active matrix arrays containing 90,000 devices (60,000 TFTs and 30,000 capacitors) were made containing only a small number of imperfections, which did not interfere with the operation of the panel.

The resulting displays clearly demonstrated the point that the use of the TFT addressing array allows the selection of an optimal display media. The displays were legible in up to 4000 fc ambients and under those conditions dissipated less than 3 mW per 5 x 7 alphanumeric character. The TFT matrix was readily interfaced to external data sources and in fact, in a related program, TFT scan and peripheral address circuits have been made that allow simple serial data input. The displays were also multifunctional and alphanumeric, graphical and real time, grey level TV imagery was displayable.

This report summarizes the program; the basic rationale behind the TFT matrix concept is detailed followed by the electrical design principles. Fabrication methods for the matrix and the complete displays are described. Finally the measured TFT and display properties are given together with a listing of related further developments now in progress.

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1. Introduction

The Army's need for a light weight, lower power solid state multi-element display is both clear and pressing. In the course of this program many specific examples have come to light; the TACFIRE and TOS programs have needs in the field terminal area (e.g. the Digital Message Device (DMD)), in forward area teletype applications (FATT), in the artillery battery control system (BCS), in the command and control area (the ICPP). Other typical Army uses could include the QCS (Query Control Station), and all forms of tactical computer terminals. The applications for Army training systems are also widespread. A portable video device would be invaluable as part of a field training and instructional device in the concepts now being developed by the Army's Office of Communicative Technology.

The utility of a solid state display in Army avionics is also evident. The need for solid state multifunctional displays in attack helicopter cockpits (e.g. in the ITACS program) is important, given the power, weight, volume and physical environment problems associated with such weapons. Many more examples could be quoted but the message is clear; the Army has a need for a multielement display concept usable in tactical situations having the following requirements:

(a) low in power dissipation to allow battery powered use for realistic lengths of time

(b) light emitting so that it is independent of the ambient light level

(c) Legible, with minimal error, in ambient brightness levels commensurate with the brightest sun-lit day

(d) Dimmable to very low levels to avoid loss of eye dark adaption

(e) Having a character font, and elemental fill factor, of sufficient quality to minimize error in reading

(f) Very low in bulk and light weight to allow use in limited space and to allow ease of carrying if hand held

(g) Rugged and strong to avoid the need for special care and to minimize breakage etc.

(h) Reliable in the field and easily replaceable by untrained personnel

(i) Usable in a wide temperature range, storable in an even wider temperature range

(j) Low in electromagnetic emissions and in susceptibility to such emanations

(k) Multifunctional, i.e. able to show all forms of alphanumeric and graphical data and video (grey level) imagery with real time non-smear output. This is important to allow a functional redundancy in a single device, and perhaps more important so that a single technology can become standard in a wide range of devices with consequent advantages in cost and in logistical simplification

(l) Able to survive the normal hazards of field use, dust, rain, immersion, shock, vibration etc.

(m) Easily electronically and physically interfaceable to modern IC logic systems

(n) Extendable to large or small areas and to low and high resolutions for the reasons given in subparagraph (k)

(o) Relatively low in cost

This gamut of properties places an unreconcilable burden on available technology and with that realization this program had its genesis.

To develop such a device means that the constraints now placed on display media by the need to provide the two key components of matrix addressing viz; cross talk isolation and elemental storage, must be lifted. To remove these constraints, and hence allow selection of a display media that can meet the above criteria, the only potential concept is to provide the matrix function in an integral electronic addressing array. As so clearly pointed out in detail in the next section, the only technology capable of meeting these objectives is the thin-film transistor addressing matrix.

This report summarizes the work done to achieve these objectives. It is our belief that the displays developed in this program come far closer to meeting the objectives than any other available or developmental technology. All the major goals of the program were met and good quality displays in all the required formats were delivered to the US Army Electronics Command.

2. Basic Principles and Electrical Design

2.1 The Active Matrix Concept

Matrix addressing of solid-state displays has been extensively used in the past, both with active and passive display media. Usually two sets of parallel busbars, orthogonal to each other, are employed with the display material sandwiched between them. These matrices can be termed "passive", since they are simply conductors of signals and power. Gain-producing, non-linear or switching and memory functions have to be provided by external circuits in combination with the electrical properties of the display medium.

There are certain inherent limitations in the use of passive matrices. These limitations relate partly to the onerous electrical performance requirements placed on the display materials and partly to the need for rather elaborate external driving circuits. The requirements placed on passive display materials include:

- Need for large non-linearities
- Uniformity of thresholds
- High speed of response
- Local storage capability, consistent with gray-scale response.

The problems related to the external driving circuits we may list as:

- Current and/or voltage requirements, particularly for fast operation
- Complexity
- Expense
- Mounting and interfacing with matrix (size disparity).

For these, and many other reasons, we adopted an approach based on the development of an "active" matrix for display addressing. Such matrices contain switching and/or memory elements at every intersection point and can, in principle, be completely integrated with the display medium. The purpose of an active matrix is to separate out the electronic functions to be performed on the display, leaving the display medium with only the optical requirements. By extension, the active matrix will ideally also incorporate those scanning, decoding and driving functions which have to be carried out at the edges of the display panel, thus eliminating the large number of external connections that otherwise have to be made to a large matrix.

It is clear that if such an active matrix can be constructed, it would provide a radical solution to the display "wiring" problem, and would be compatible with a wide variety of display media. Then the medium could be chosen for its optical characteristics, while the electrical functions would be taken over by the matrix.

The question arises then as to a suitable technology for the construction of such matrices. As early as 1968, we developed and reported on a high-voltage thin-film transistor suitable for switching conventional ac-EL phosphor lamps. It became evident to us that the construction of large-area active matrices was a natural task for thin-film technology.

The thin film transistor in its modern form can be traced back to the work of Weimer et al at RCA. It is of course an <u>all evaporated</u> field effect transistor analogous in operation to the now

conventional MOSFET. The devices upon which this work is founded are based on CdSe as semiconductor and therefore are n type. They can be made in enhancement and depletion modes and are constructed as shown in Fig (1). Note the double gated structure which results in much improved device gain. Specific results on the TFT, its properties etc., are given in Section (4.4) below.

The advantages of thin-film technology in this application over its nearest rival, silicon LSI technology, can be summarized as follows:

- o ability to cover the large areas required for any useful display;
- o availability of high-voltage FET's;
- o uniformity over large areas (many square inches);
- o simplicity of technology;
- o complete integrability with a variety of display media;
- o suitability for peripheral circuitry (scanners, decoders, line drivers, line memories),integrable with TFT matrix;
- o potential for completely automatic fabrication.

The validity of this comparison is evident by the fact that, despite efforts, no display comparable to the ones reported here has ever been made with silicon technology.

2.2 Electrical Design

In this section we discuss the operation of the matrix and performance requirements imposed on the TFT devices as dictated by the requirements of the display panel operating at a 60 Hz refresh.

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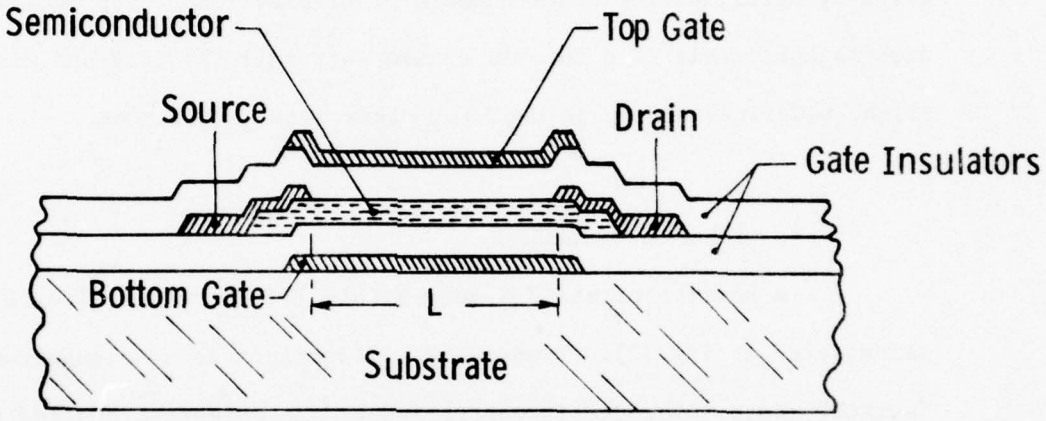


Fig (1) Cross section of TFT (schematic)

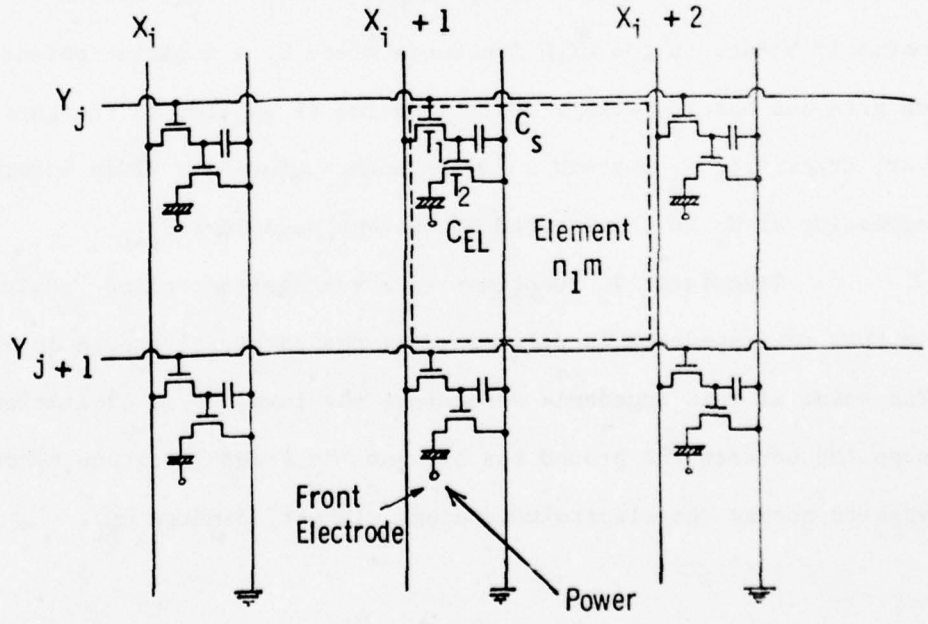


Fig (2) The elemental circuit at each picture element

Particular attention is given to device uniformity and stability requirements in relation to panel reliability. Long term (life) performance characteristics of the thin-film transistors is detailed in Section 4.4. The analysis is applied to a 120 line display but is easily generalized for other numbers of display lines. In addition the data is applicable to a 50 mils square unit cell (20 lpi) but with slight modification can be used for other line resolutions.

2.2.1. The TFT-EL Matrix

A portion of the X-Y addressable TFT-EL matrix circuit is illustrated in Fig (2). Transistor T_1 functions as a voltage-controlled "switch" whose impedance is controlled by the potential applied to the gate bus bar Y_J. The drain electrode of T_1 is connected to bus bar X_i and its source to element storage capacitor C_S. This switch is normally biased in the high impedance state by a negative potential on gate bus bar Y_j, when a positive pulse is applied to the gate bus bar, transistor T_1 assumes a low impedance state and video information appearing at X_i is transferred to storage capacitor C_S.

Transistor T_2 functions as a voltage-controlled "resistor", in that its impedance is determined by the potential stored on C_S. The value of this impedance determines the level of ac excitation, supplied between the ground bus bar and the front electrode, which appears across the electroluminescent element, denoted C_{EL}.

2.2.2. Line-at-a-time Addressing

In contrast to normal "raster" type addressing in which each element in the display field is scanned in sequence at megahertz rates, line-at-a-time addressing permits the display of video information at say, 60 Hz refresh, but with only modest performance requirements imposed upon the TFT devices. The line-at-a-time addressing scheme is illustrated in Fig (3). With this method video signals for an entire line of display elements are first stored sequentially in an external shift register. The outputs of this register are supplied to the display panel on the vertical information buses (X_i) and transferred to the corresponding element storage capacitors, all at one time, when a switching pulse on the selected horizontal bus (Y_j) closes all the element signal gates in that line. Introduction of the intermediate storage register relaxes the bandwidth requirements of the display element signal gates, as well as that of the information buses, by a factor approximately equal to the number of elements in a display line.

The vertical scan frequency is 60 Hz and thus each horizontal line is refreshed every 16.7 ms. The register cycle period is 127 μs, one-half this period being allocated for entering sampled information into the register and the other half for transferring the information levels to the storage capacitors in a given line on the display panel.

The following sequence of events describes the complete line-at-a-time addressing process:

(1) Sample brightness information at a 2 MHz rate for 60 microseconds and enter in all 120 register stages.

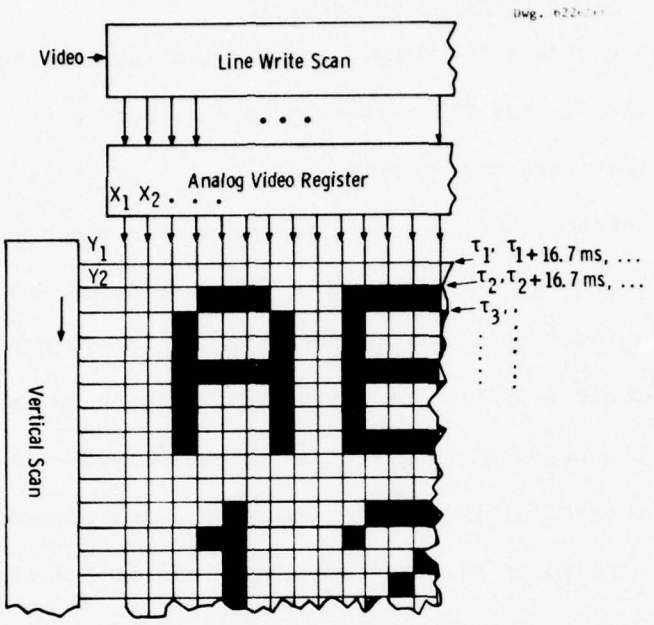


Fig (3) Line at a time addressing

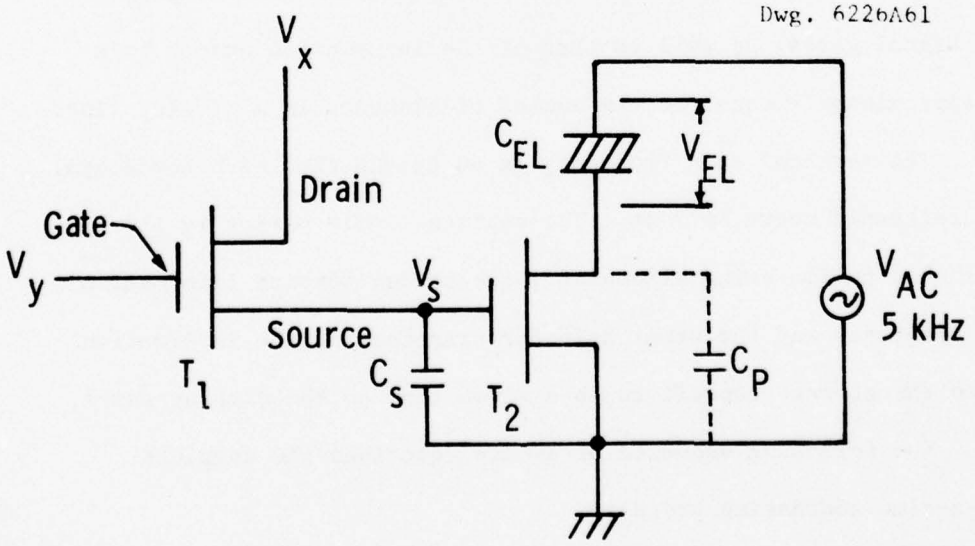


Fig (4) Real elemental pixel circuit including parasitic capacitance

(2) Disable sampling circuit and apply a 60 microsecond switching pulse on the corresponding horizontal bus (Y_j). This transfers stored potential levels from vertical information buses (X_i's) to the element storage capacitors (C_{sj}'s).

(3) Sample brightness information for the next horizontal line and continue the sequence until the whole field is stored.

2.2.3 TFT Performance Requirements

The "true" circuit schematic associated with each elemental picture "point" is given in Fig (4). The video storage capacitor C_s, connected between the gate and source of T_2, has a capacitance of 20 pf. At an excitation frequency of 10 kHz, the electroluminescent element can be modeled as a pure capacitance (C_{EL}) of value 8 pf. Under the 30 lpi condition the C_s value is 15 pf and the EL capacitance 1.5pf (single level) and 3.5 pf (double level). The parasitic capacitance, C_p, appearing in the drain circuit owing to gate overlap, etc. is approximately 0.1 pf. The power bus supplies a 150 volt (p-p) ac signal at 10 kHz to the panel. The typical brightness response as a function of applied ac potential (at 10 kHz) for the E.L. element is shown in Fig. 5.

In simplest terms, the function of T_1 is to transfer the potential V_x appearing at its drain electrode to the storage capacitor C_s, whenever the gate potential V_y is positive. The potential V_s stored on C_s then controls the conduction level of

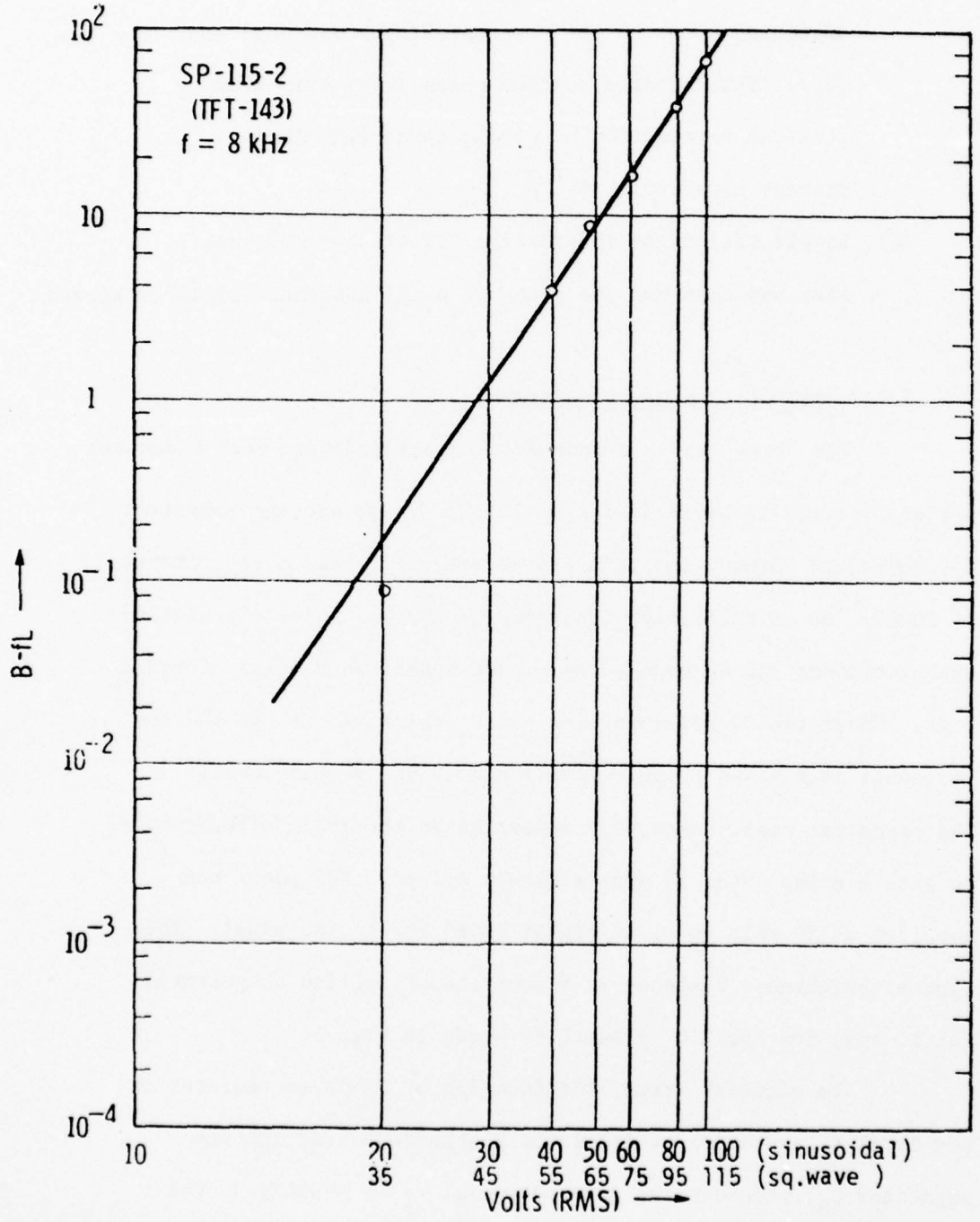


Fig (5) Phosphor brightness as a function of ac-potential

T_2, which in turn modulates the effective ac potential across C_{EL}. The ON impedance of T_1 (operating in the "linear" region) is determined by the instantaneous gate-source voltage, $V_y - V_s(t)$, through the relation

$$R_{ON}(T_1) = \left\{ \frac{Z\mu C_i}{L} \left[V_y - V_s(t) - V_T \right] \right\}^{-1} \qquad (1)$$

where Z = channel width of the TFT

L = channel length of the TFT

μ = carrier mobility in the semiconductor

C_i = gate-insulator capacitance per unit area

V_T = threshold voltage.

The differential equation governing the video transfer is

$$\frac{dV_s(t)}{dt} = \frac{Z\mu C_i}{LC_s} \left[V_x - V_s(t) \right] \left[V_y - V_T - V_s(t) \right] \qquad (2)$$

where we have made use of eq. (1). The solution is given by

$$V_s(t) = \frac{V_\Delta (V_x - V_{so})\, e^{-t/T}}{V_\Delta + (V_x - V_{so})(1 - e^{-t/T})} \qquad (3)$$

where $V_\Delta = V_y - V_x - V_T$

and V_{so} = the initial value of potential stored on C_s at t = 0.

The time constant T is related to the effective ON resistance of T_1 as

$$T = R_{eff}\, C_s = \left(\frac{Z\mu C_i}{L}\, V_\Delta\right)^{-1} C_s \qquad (4)$$

Owing to the differing values of V_s stored on C_s, the effective charging resistance R_{eff} will vary, depending upon whether the video (V_x) is changing from light to dark (ON → OFF) or from dark to light (OFF → ON). To illustrate this effect the following typical values are assumed:

$$\text{video} = \begin{Bmatrix} \text{ON} \\ \text{OFF} \end{Bmatrix},\ V_x = \begin{Bmatrix} +10 \\ 0 \end{Bmatrix},\ V_y = \begin{Bmatrix} +20 \\ +20 \end{Bmatrix},\ V_{so} = \begin{Bmatrix} 0 \\ +10 \end{Bmatrix}$$

Additionally, it is assumed that T_1 has a threshold voltage (V_T) of +2 volts. Using the above values, eq. (3) is solved for the time constant T required to achieve a given video transfer, expressed as a percentage of ΔV_x, in the 60 μs line dwelling interval. Using these values of T, the effective ON resistance R_{eff} is calculated from eq. (4), and the results plotted graphically in Fig. 6. Notice that the requirements on R_{eff} vary by nearly a factor of two, depending upon the direction of video change.

During the remaining 16.64 ms of the frame period when the other vertical lines are being scanned, T_1 must remain off to prevent C_s from discharging its video signal V_s. In this mode T_1 can be

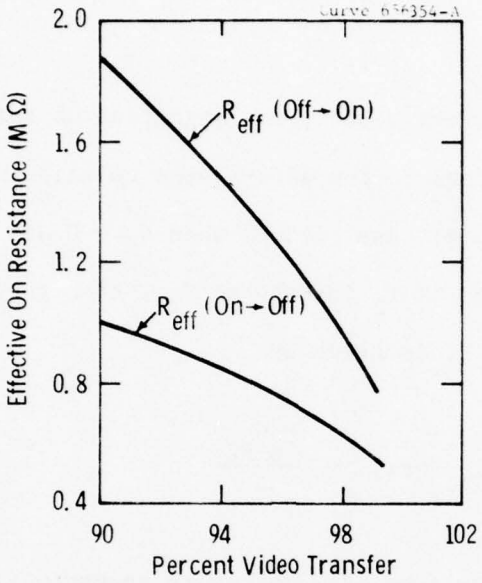


Fig (6) Video transfer efficiency vs effective on resistance

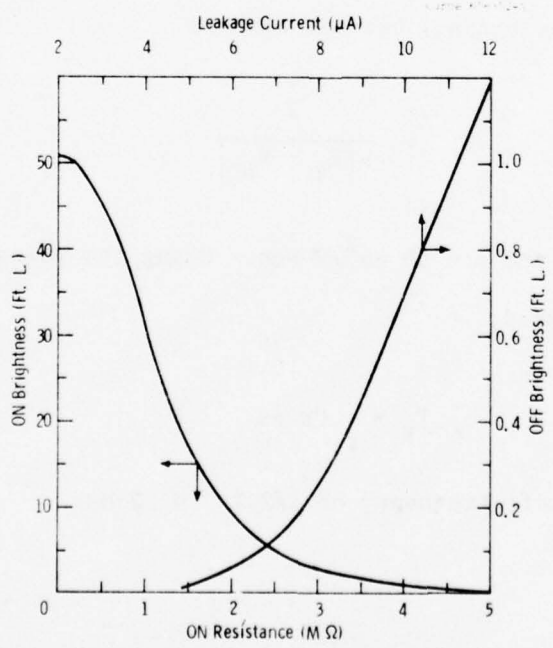


Fig (7) Element brightness as a function of T_2 ON/OFF resistance

modeled simply as a current source, the magnitude of this "leakage" current being proportional to the gate-source voltage in the OFF state. Clearly the "worst case" occurs when $V_s = 0$ and $V_x = +10$ V. If the threshold voltage of T_2 is denoted V_{T2}, then the maximum OFF leakage current of T_1 is given by

$$I_{L1}(\max) = \frac{C_s V_{T2}}{\Delta t} \tag{5}$$

which for a threshold voltage of 2 volts, is approximately 2.5 nA.

With respect to the switching speed of the TFT, we require a turn-on time which is short compared to the 60 μs line dwell time. From FET theory, the channel transit time is

$$T_t = \frac{L^2}{\mu |V_x - V_{so}|} \tag{6}$$

where L = 2.5 mils and $\mu \approx 50$ cm^2/V-sec. Using the values of V_x and V_{so} previously assumed,

$$T_t = .08 \text{ μs}$$

which implies a cutoff frequency of $1/2\mu T_t = 2$ MHz.

The fraction of the 150 V (p-p) 10 kHz signal appearing across the electroluminescent element (C_{EL}) is determined by the ON resistance of T_2. Its on resistance as a function of the video signal V_s is given by

$$R_{ON}(T_2) = \left\{ \frac{Z\mu C_i}{L} \left[V_s(t) - V_T \right] \right\}^{-1} \tag{7a}$$

for the positive half-cycle of the ac signal, and

$$R_{ON}(T_2) = \left\{ \frac{Z\mu C_i}{L} \left[V_s(t) + |V_{AC}| - |V_{EL}| - V_T \right] \right\}^{-1} \tag{7b}$$

for the negative half-cycle. Equations (7a) and (7b) are valid only for the regions where the source-drain voltage is much less than the saturation voltage, $V_{DS}(sat)$. Beyond saturation the TFT behaves as a voltage-controlled current source.

An exact solution for the resulting ac component appearing across C_{EL} results in a rather formidable boundary value problem and thus only approximate solutions will be considered further. If we denote the effective on resistance of T_2 as R_2 then the magnitude of the ac signal appearing across C_{EL} is given approximately by

$$|V_{EL}|_{ON} = \frac{|V_{AC}| \cdot (1 + \omega^2 R_2^2 C_p^2)}{\sqrt{(1+\omega^2 R_2^2 C_p C_{EL})^2 + \omega^2 R_2^2 C_{EL}}} \tag{8}$$

where ω is the radian ac frequency and C_p is the parasitic circuit capacitance.

When T_2 is turned "off" we have the equivalent of a current source representing the off-leakage current, I_{L2}, in parallel with C_p. Under these conditions

$$\left|V_{EL}\right|_{OFF} = \frac{1}{C_{EL}} \left[\left|V_{AC}\right| . C_p + \int_{t_{off}} I_{L2}\, dt \right] \qquad (9)$$

where t_{OFF} represents the interval during which T_2 is OFF.

In Fig. 7 is shown the resulting brightness of the E.L. element when T_2 is in the ON or OFF state. The left-hand curve represents the ON brightness vs the effective ON resistance R_2, as determined from eq. (8) and Fig. 5. The right-hand curve represents the OFF brightness owing to both the effects of parasitic capacitance C_p and OFF-leakage current I_{L2}, as determined by eq. (9) and Fig. 5. As can be seen in Fig. 7 the grey scale is essentially only a function of R_2(ON), while the ON-OFF contrast ratio depends upon both the ON resistance and the OFF-leakage current.

2.2.4 Stability Requirements

The requirements on TFT stability depend upon the mode in which the display panel is operated; the stability tolerances being more severe for a panel operated with grey scale than for one without grey scale. Variations in T_1's parameters effect the video signal V_s stored on C_s, while variations in T_2's parameters effect the ac excitation appearing across C_{EL}. To see the effects of drift in TFT characteristics on the resulting output (EL brightness) of the panel, the acceptable ON-OFF brightness limits are arbitrarily placed at

$$B\ (ON) \geq 15\ \text{ft-L}$$

and

$$B\ (OFF) \leq 0.15\ \text{ft-L}$$

which implies a worst case contrast ratio of 100.

From Fig. 7 the resulting limits on T_2 (based on the above brightness values) are $R_2(ON) < 1\ M\Omega$ and $I_{L2} \leq 8.5\ \mu A$. Also from Fig. 7 the maximum practical brightness is 25 ft-L, which occurs for $R_2(ON) \simeq 200\ K\Omega$. The slope of the ON-brightness vs ON-resistance curve in the region of 15 ft-L is roughly 15 ft-L/MΩ. The factor $(Z\mu C_i/L)$ has a value of approximately 1×10^{-6} mho/volt for both T_1 and T_2. If we assume a worst case video transfer of 90%, then V_s has a minimum value of + 9 volts in the ON state. This requires that T_2 have a threshold voltage no greater than + 8 volts (as determined from eq. 7a) in order to maintain $R_2(ON) < 1\ M\Omega$. While from a stability standpoint it might be argued that T_2 should be designed with a low threshold voltage, there is a tradeoff between threshold "noise margin" and allowable leakage current I_{L1} of T_1, as determined from eq. (5).

Stability requirements on T_1 relate directly to its effective ON impedance R_{eff}. As evidenced by Fig. 6, the worst case situation occurs when T_2 is being switched from ON to OFF. For ON-OFF operation of the panel (without grey scale), a 90% video transfer would be adequate, whereas for operation with grey scale, a transfer of at least 95% is needed. The maximum limits on R_{eff} for

these two cases are 1 MΩ and 750 KΩ, respectively. Assuming the latter as a worst case value,

$$V_{\Delta}(\min) = \frac{L}{Z\mu C_i} \cdot \frac{1}{R_{eff}(\max)} = 1.3 \text{ V}$$

Using the values listed in the previous section, this translates to a maximum threshold voltage for T_1 of + 8.7 volts. Thus for operation without grey scale both T_1 and T_2 can tolerate shifts in threshold voltage by as much as + 6 volts, assuming both had initial threshold voltages of + 2 volts.†

The effect of T_2's threshold stability on grey scale response can be approximated by the relation

$$\frac{dB}{dV_{T2}} = \frac{dB}{dR_2} \cdot \frac{dR_2}{dV_{T2}} = \frac{L}{Z\mu C_i (V_s - V_{T2})^2} \cdot \frac{dB}{dR_2}$$

or

$$\frac{dB}{dV_{T2}} \simeq \frac{15 \text{ ft-L}}{R_2(V_s - V_{T2})} \qquad (10)$$

where R_2 is in MΩ.

†It should be pointed out that these values are somewhat arbitrary, in that bias levels can be varied to adjust for slight variations in transistor characteristics from different panels.

2.2.5 Uniformity Requirements

The requirements on device uniformity follow along similar arguments as those imposed by stability requirements. Again the most stringent tolerance requirements are imposed upon T_2 when grey scale operation is desired. Non-uniformities in T_1 are tolerated to the extent that the video transfer from V_x to V_s is not appreciably deteriorated or that the OFF-leakage current is not above that imposed by eq. (5). For ON-OFF operation without grey scale, non-uniformities in T_2's ON resistance will have a negligible effect on panel operation so long as $R_2(ON) < 1\ M\Omega$. The penalty is, of course, that those devices with R_2 near 1 MΩ will have a lower stability "noise margin".

Table 2-1 summarizes the electronic specification resulting from this analysis.

Table 2-1

Summary of Electrical Requirements

Device	Parameter	Requirement	Achieved
T_1 logic TFT	I_{ON}	> 100 μA	300 μA
	R_{ON}	< 0.1 MΩ	30 kΩ
	I_{OFF}	< 2.5 nA	1.0 nA
	V_B*	> $50V_{pp}$	>>$50V_{pp}$
T_2 power TFT	I_{ON}	> 125 μA	350 μA
	R_{ON}	< 0.8 MΩ	~100 kΩ
	I_{OFF}	< 7 μA	1 μA
	V_B	> $200V_{pp}$	$300V_{pp}$

*Breakdown limit

3. The Development of Fabrication Methods

3.1 Introduction

As we have seen each elemental cell will need to contain the following elements:

(a) A logic TFT (T_1)

(b) A power TFT (T_2)

(c) A storage capacitor C_s

(d) An output pad for the EL lit area

(e) Interconnections between those elements in a cell

(f) A gate bus connecting all the cells in a row

(g) A source bus connecting all the cells in a column

(h) A power bus connecting all the cells in a column

(i) External contacts at the edge of the panel to all the buses.

In addition the TFT circuit must be isolated from the ac potential across the phosphor. Finally a top continuous ground electrode must be provided.

This is unquestionably a formidable fabrication problem when one considers the dimensions and number of cells involved. The three formats used in this program were, in chronological order

6" x 6" 20 lpi (12,000 elements)

6" x 6" 30 lpi (25,000 elements)

6" x 6" 30 lpi (17,000 elements)

Note that there are some edge losses in the 6" x 6" cell to allow for contacts so that the actual active display area was approximately 5.5" x 5.5".

The major achievement of the program lies in the fabrication of these matrices. The following section describes the methods and procedures used.

3.2 The TFT Circuit Fabrication Process

A number of techniques are possible candidates to obtain the thin film circuit patterns described above, bearing in mind the need for good uniformity over a 6" x 6" area and that the process should be ultimately adaptable to mass production techniques. Photoresist methods well known to solid state technology are available which, combined with evaporated or silk screened conductors, could achieve the objective. However photoresist techniques over large areas such as 6" x 6" are far from easy and on an eventual mass production basis would require complex and expensive processing. Silk screening, and thick film photosystems, generally have too poor a resolution for our purposes although combining these methods with evaporated active devices could be used. Experience has shown, however, that the less the contamination introduced into the system through the use of 'wet' techniques, the better the life and performance of the TFT.

Evaporation through fixed "dedicated" masks is a real possibility. The whole circuit could readily be fabricated in this fashion. Indeed, this is the approach we intend to pursue in our pilot manufacturing program for these panels. It does, however, require a large vacuum system to accommodate all the necessary masks, and thus avoid the need for repeated pumpdowns.

3.2.1 The Movable X-Y Masks Method

The repetitive nature of the matrix circuit opened the door to a concept that not only solved the problems described above but also becomes a pattern generating method applicable to a wide variety of alternative circuits: i.e., a universal deposition-system for the repetitive large area circuits typical of matrix displays. This idea is to generate the desired pattern by the controlled movements of a set of two thin metal masks placed in contact with each other and the substrate. Such masks (6" x 6") were fabricated having square openings as illustrated in Fig (8). Through movements in the masks, almost any desired rectangular pattern could be generated, as shown in Fig (8). Continuous lines, such as the bus bars, were easily fabricated by lateral movements to create overlapping regions. After much experimentation it was found that 3 mils thick, 6" x 6", nickel-coated Be-Cu masks were the best; the apertures were 25.0 mils in size on 50.0 mils center to center spacings. The masks were mounted in frames and the mask frames mounted in movable micrometer controlled assemblies. An assembly is shown in Fig (9). Masks and glass substrate are mated in the assembly which is fitted with a large magnet placed on top of the glass substrate so as to pull the two masks into contact with themselves and the substrate.

To generate a complex set of patterns the following method was established. The mask set, in the controllable frame assembly, was placed under a NIKON 6C large area shadowgraph. This presents a magnified area of a small portion of the masks in transmitted light. The masks were moved to achieve the required rectangular pattern and the readings on the micrometers recorded. The patterns are compared to a

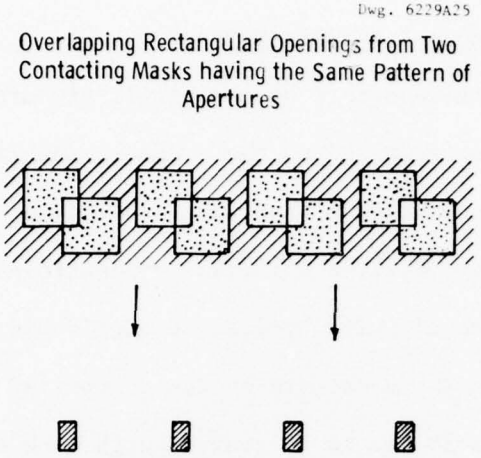


Fig (8) The principle of the X-Y approach to TFT matrix fabrication

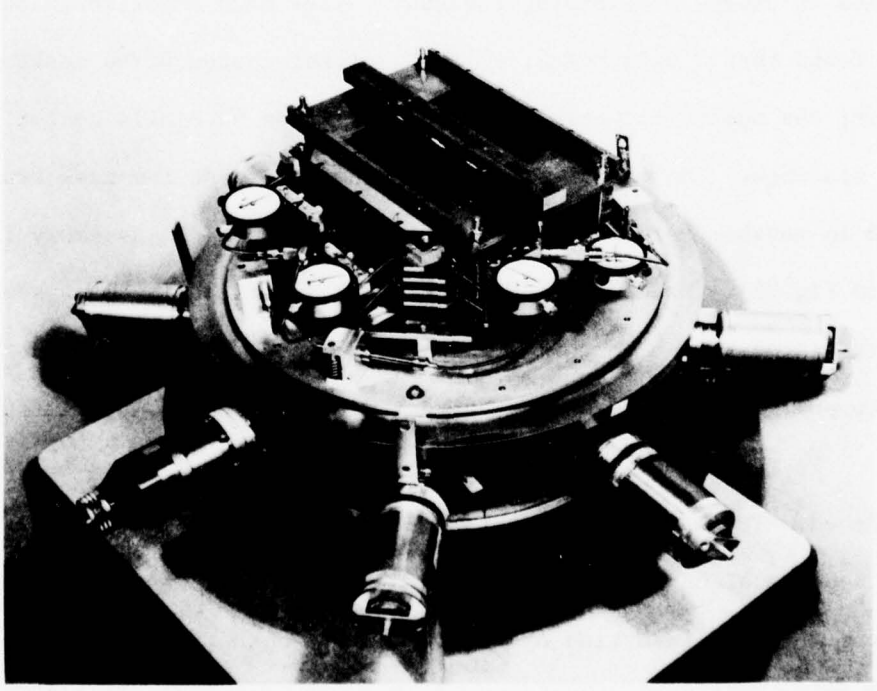


Fig (9) The X-Y deposition jig

master layout on transparent sheet overlayed on the shadowgraph screen. Fig (10) shows a typical layout. This was then repeated for each desired opening configuration, about 30 in all. Resetting the four positioning dial micrometers to the pre-established values then regenerates that rectangular pattern. Since the masks were of excellent uniformity over their whole area, having been made through step and repeat photomasking methods, this particular pattern was then created over the whole 6" x 6" area, at each of the 12,000 elemental points. This, of course, requires good initial mask to mask alignment - a condition that was readily checked through shadowgraph examination of the generated patterns at various parts of the 6" x 6" area prior to positioning in the vacuum system. Feed throughs made in the vacuum system allowed control of the micrometers during the deposition process.

The evaporation system itself (Fig 11) was conventional, although rather elaborate. The height was extended to allow insertion of the masking jig and its feedthroughs, and to position the substrate 33" from the evaporation sources. At this distance the coverage of a 6" square area is sensibly uniform. The large throw distance did produce an undesirably rapid accumulation of material on the bell jar walls and frequent cleanups were needed.

Monitoring of the various depositions was accomplished through SLOAN crystal oscillators calibrated by deposition and thickness measuring (TALYSTEP) runs. Thermal evaporation was from an oxide coated tungsten basket and electron beam evaporation was from intermetallic crucibles or graphite crucibles fitted in copper hearths. The EB gun was an AIRCO TEMESCAL STIH-270-2 system.

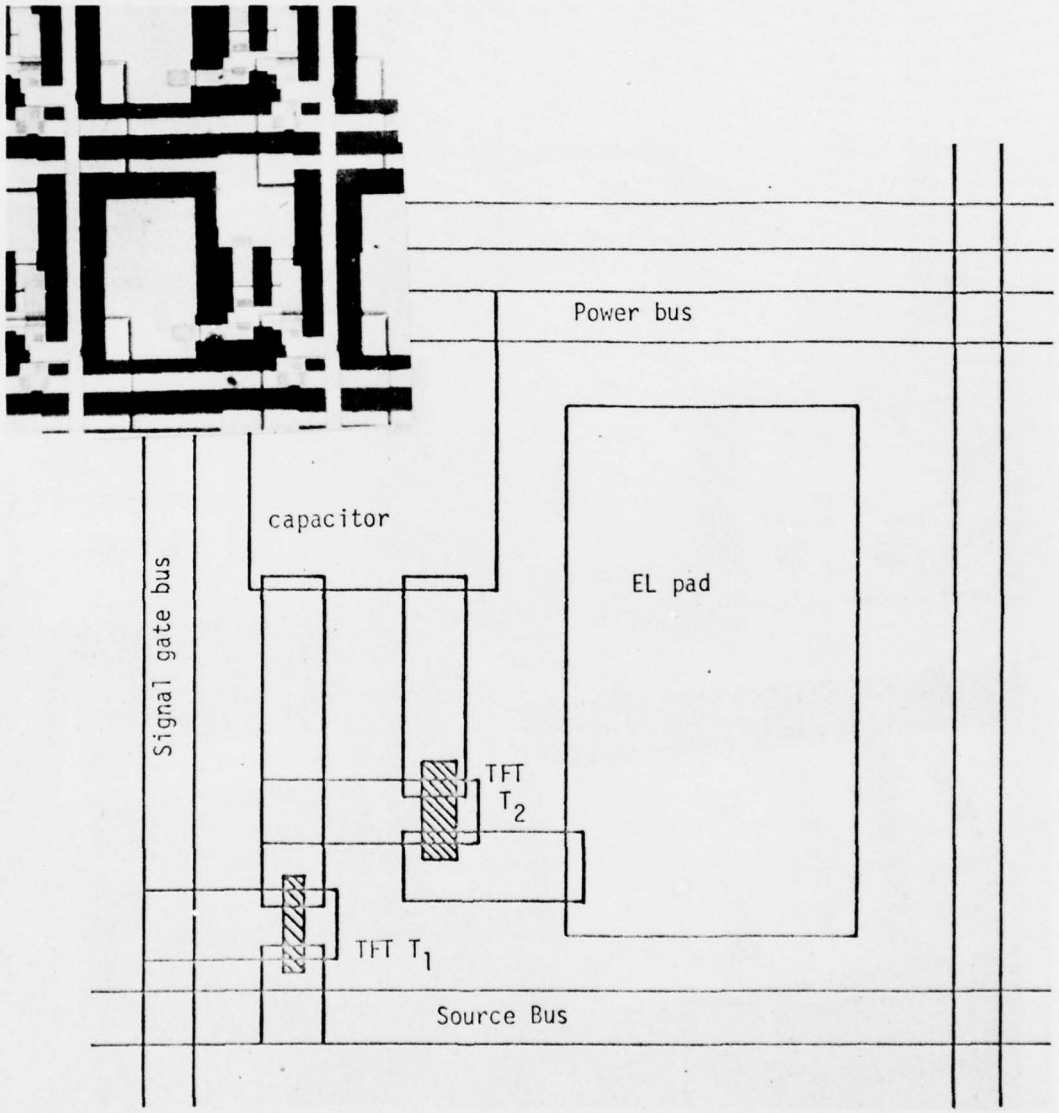


Fig (10) Typical layout for pattern registration

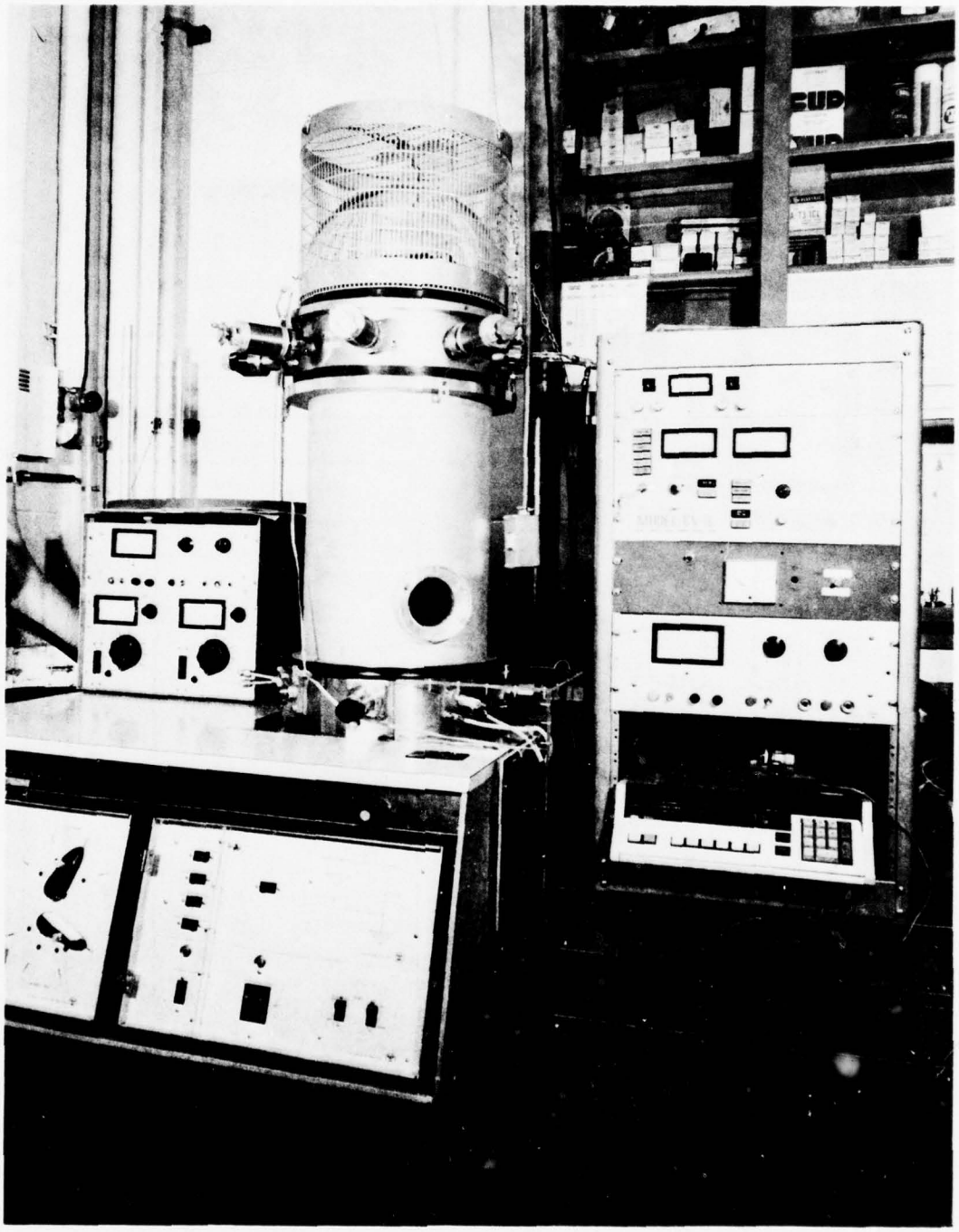


Fig (11) The vacuum deposition system

All evaporations were conducted at pressures below 5×10^{-7} torr achieved by overnight pumping.

3.2.2 Thin Film Material Selection for TFT Matrix Fabrication

Considerable research at the Westinghouse R&D Center has been conducted in recent years toward optimizing the selection and deposition of materials suitable for stable, low leakage TFT's with good transconductance (g_m). As we have seen above, leakage levels of a few nanoamps are required for operation of the panel. Our work on previous TFT programs has established that CdSe is an excellent semiconductor for these applications. Other materials (CdS, CdTe) have been examined, but CdSe gave the most stable, highest gain devices. The source and drain must make ohmic contact with the semiconductor. A good conductor having good glass adhesion was also required for the source material, since it is integral with the column (X) bus bar. Aluminum, chromium/gold double layers, indium/gold layers, and copper were among the more successful materials examined. Al gates were found the most stable with sapphire (Al_2O_3) as the gate insulator (5000 Å). Al_2O_3 insulator was also deposited at the bus bar crossover points between the metal layers and in the capacitor layers. The glass substrates were 48 mils thick Corning 7059 glass; the low alkali glass avoids TFT contamination. Typical thin film transistors and matrix elements pictured at high magnification and with explanatory drawings, are shown in Fig. (12) and Fig (13) and (14). Fig (15) shows a complete TFT matrix Table 3-1 summarizes the optimum process sequence and device fabrication recipe for the entire matrix. Details of the TFT performance are given in Section 4.4.

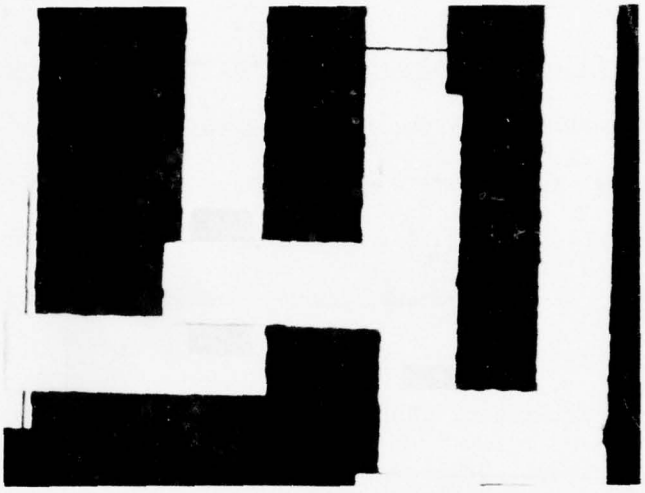


Fig (12) A typical TFT at high magnification

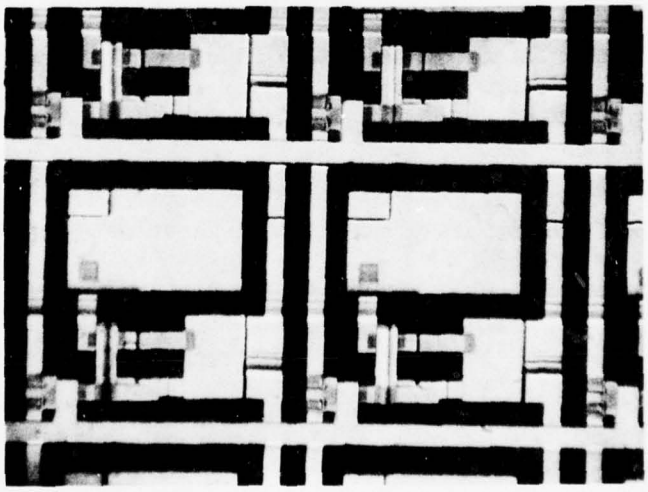


Fig (13) A section of a TFT matrix

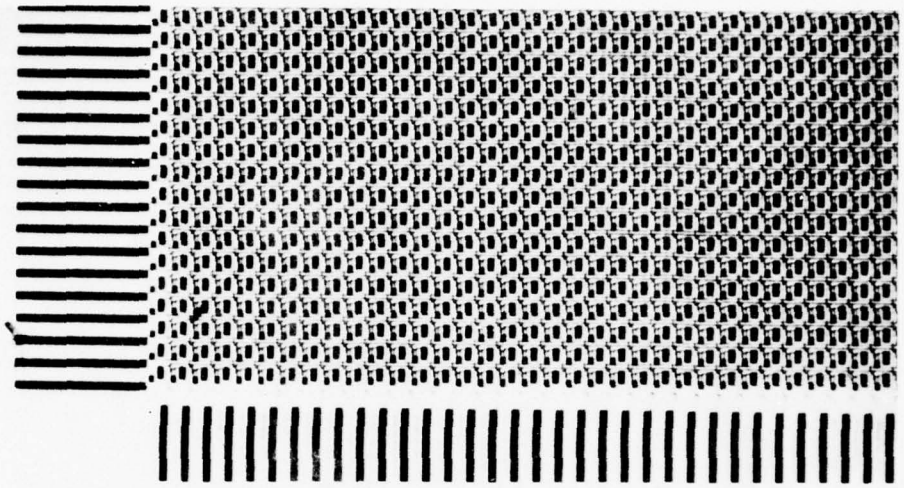


Fig (14) A larger section of TFT matrix

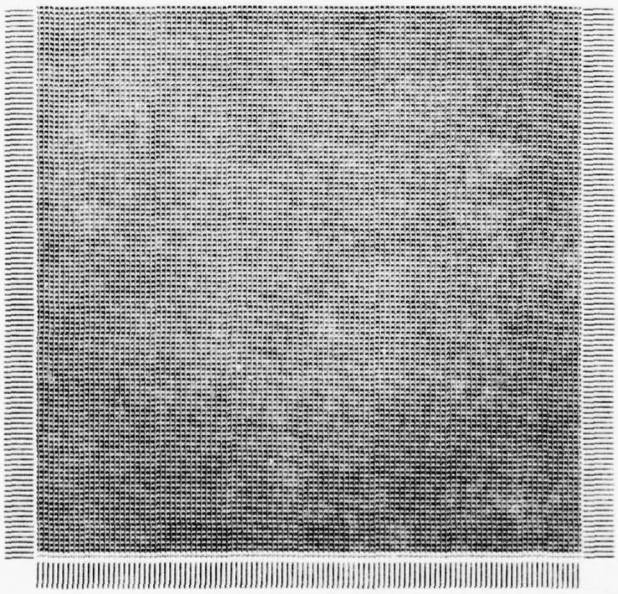


Fig (15) A complete TFT matrix

Table 3-1

Summarized Deposition Sequence
30 lpi Display

1. Source bus - 3 positions, Al-1000 Å
2. Gate transistor 1 - Al 500 Å
3. Gate transistor 2 - Al 600 Å
4. Cap Interconnect - Al 600 Å
5. Power Bus - 2 positions, Al - 1000 Å
6. Cap - Al 600 Å
7. Transistor Gate Insulator - Al_2O_3, 7000 Å
8. Semiconductor CdSe 80Å
9. Source 2 evaporations: In 100 Å, Cu 1000 Å
10. Drain 2 evaporations: In 100 Å, Cu 1000 Å
11. Interconnects 2 positions - Cu 700 Å
12. Insulator Gate #1 Al_2O_3 7000 Å
13. Insulator Gate #2 Al_2O_3 7000 Å
14. Semiconductor #2 CdSe 100 Å
15. Doping layer In 5 Å
16. Source #2 2 evaporations In 100 Å, Cu 1000 Å
17. Drain #2 2 evaporations In 100 Å, Cu 1000 Å
18. Interconnects 2 positions Cu - 700 Å
19. Insulator Gate #2 Al_2O_3 7000 Å
20. Cap Insulator Al_2O_3 7000 Å
21. Gate #2 Al 600 Å
22. Gate Interconnect Al 600 Å

Table 3-1 (Continued)

23. El Pad Al 1000 Å
24. Gate #1 transistor Al 600 Å
25. Interconnects 2 positions Al 600 Å
26. Capacitor Al 600 Å
27. Cover insulator Al_2O_3 1000 Å
28. Edge contacts Cr 200 Å, Au 1000 Å

3.2.3 Summary of Key TFT Process Developments

The significant experimental insights that led to displays of good quality are perhaps the heart of the programs. However when listed they appear among the most mundane! In fact the basic concept remained the same throughout the bulk of this program, only the detail changed.

The most significant process detail was the realization that the cleanliness of the glass was of prime importance. Elaborate glass cleaning methods were developed, the most critical factor being the use of vigorous physical scrub action rather than relying on a simple chemical action. The other important ingredient in glass cleaning was the use of Millipore$^{(R)}$ filtered "Super Q" water for final rinse. Great care in handling the glass was important as was the development of consistent glass drying methods.

Mask cleaning was also important, firstly it was necessary to clean the masks as received (triple distilled methanol), secondly after two deposition run sequences (an average) the mask set built up so much material that it required cleaning. The cleaning technique (involving a rejection-type process) is shown in Fig (16). Detailed visual inspection of the masks by reflected and transmitted light was essential.

Mask stretching and attachment to the frame was difficult. The eventual answer was to cool the mask and frame, stretch the mask on the frame when both are cold using double stick tape. When the assembly warmed up the mask was pulled taut. The major difficulty here was removing the complete residues of the tape adhesive in mask

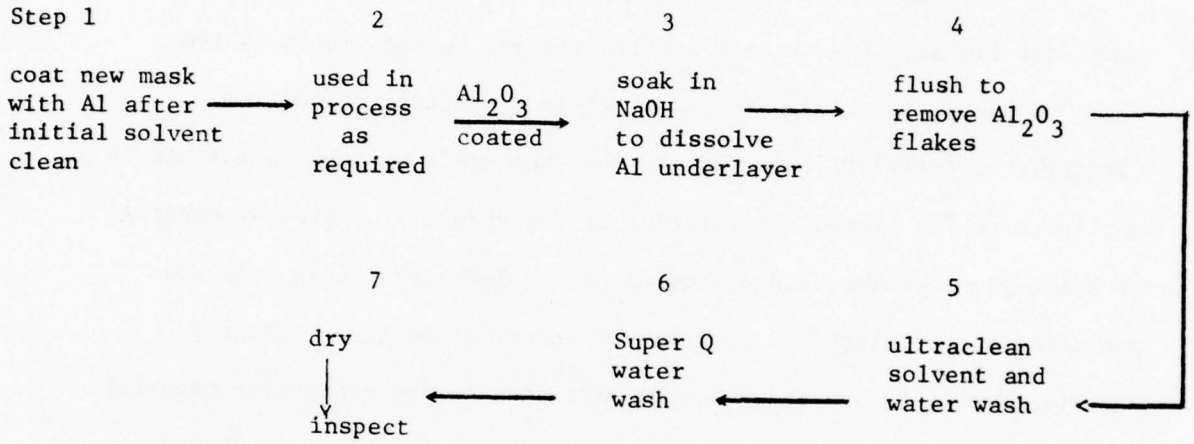


Fig (16) The mask cleaning process

cleaning. In prealignment (mask to mask) the key was good initial alignment on the shadowgraph and then placing the magnet and substrate holder on the jig and exercising it a few times. The alignment is then rechecked. Any deviation requires that the jig be examined (pin parallelism for example) to work out deviation inducing effects.

The jig system is then sealed, (all the above steps being done in a laminar flow tunnel) and transferred to the vacuum system.

Several factors are important in the actual deposition. Firstly, the turbulent pump-down of the chamber (roughing) causes minute particles to fly around the interior of the chamber. A gradual opening of the high-vac valve, and a closing of the X-Y mask set in pump down was found to be important. During the actual deposition a clearly important variable was the adequate melt down of the dielectric material; sapphire was the best source for Al_2O_3 but it was critical to de-gas in the molten condition for adequate periods. Wide sweep scan initially followed by a narrow scan covering only the central 'pool' of Al_2O_3 was the best technique. Of course following standard vacuum thin film practices was important; establishing uniform rates of deposition, avoiding interrupted cycles and crystal variation. Monitoring of input voltage to the gun , instantaneous rates, and cumulative build up, were monitored, as of course was chamber pressure.

The metal depositions required less care than the dielectric but still required good premelt and outgas. No sweep on the guns was needed with metals. Optimum methods for CdSe and indium were easier to implement and conventional resistance heated sources were used.

Replacing the CdSe at each run helped reproducibility as did the development of consistent methods to fill the hearths, the avoidance of any contamination in the materials and chamber. Another important point was preventing the peeling of chamber walls and jigs; any trace of "peel" can drop into the e-beam melt and cause a burst of material whose impact far exceeds the actual drop-in material itself.

Anneal of the circuit, [350°C, dry N_2 10 hrs] is important; key parameters are the exclusion of trace O_2 and uniformity of the heat and N_2 flow.

Circuit test looked to be a formidable problem in initial planning. However it transpired that a relatively small number of tests were sufficient to characterize the circuits. Individually probed TFTs were examined, usually about six to eight areas of the display being tested. Tests for ON current, leakage or OFF current, voltage handling, fast trapping, off leakage stability and inter/intra cell contact resistances were quickly measurable with a three or four point probe and a TEK 576 Curve Tracer. Bus bar impedances (from chrome-gold contact) could also be selectively tested in this fashion. The critical check for shorts consisted of shorting together (with a conductive rubber strip) all the gates (say) and scanning down the other contacts with a VOM-high and low resistance shorts were marked. The former usually were indications of shorts through a TFT. On some easily identifiable shorts it was possible to electrically blow the short with the curve tracer, providing the surround was grounded. Electrical opens were also identifiable through edge to edge scans of the busbars although here the check is of course for

open circuits. A few could be patched but this was not a technique to rely on.

To conclude, the fabrication of high quality TFT matrices represents a major achievement and an advancement in the state of thin film technology. No major innovations were necessary it should be noted but the skilled and systematic application of good engineering analysis and key insights as to which are the critical parameters and which are not. We believe that the present techniques, that have reduced the defect level in the best circuits to about 0.004% is extendable to zero without resort to alternate concepts. This point is amplified in more detail in Appendix III.

3.3 Display Assembly Process

The subsequent processing of the thin film matrix through to the completed display was thoroughly investigated. A definitive laboratory process was established that successfully accomplishes the following:

1. Provides a passivating inert coating over the active portions of the thin film circuit.

2. Insulates the thin film circuit, except the actual pad of the lit area of each cell and the edge contacts, from the high frequency ac EL phosphor drive voltage.

3. Coats the circuit with electroluminescent phosphor in a simple but reliable method.

4. Provides a top electrode that is continuous, transparent, and has a suitable external connection.

5. Provides hermetic packaging of the phosphor and environmental stability by a final seal process.

After the thin-film circuit fabrication, the process comprises four main steps: (I) the thin film circuit insulation, (II) the phosphor deposition and related areas, (III) top electroding, and (IV) the final seal. These steps are described in the following paragraphs.

3.3.1 Step I: Thin Film Circuit Insulation

The photoresist laminator is first set up (see Fig (17)); the temperature is set to 210°F and then left for 15 min. The tested and approved thin film circuit is then cleaned with ionizing air and brush,

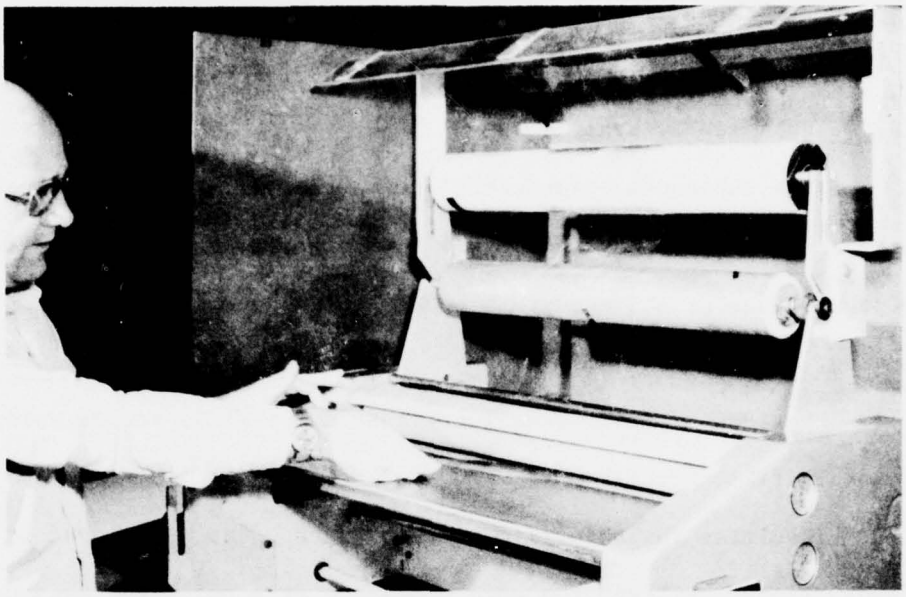


Fig (17) The photoresist laminator

Fig (18) The exposure unit

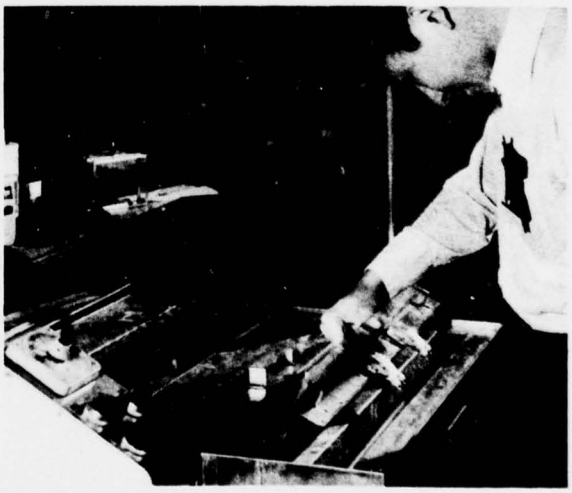


Fig (19) The developer

and is laminated with laminar photoresist material between the pressure rollers. Extraneous material is then cut off and the coated circuit examined for ripples, bubbles, and other imperfections. If not passable, the photoresist material can be peeled and the circuit relaminated.

This process has proved reliable and is capable of production rates far in excess of our needs. The major study variables here involved establishing fixed parameters for roller pressure timing. Our present optimal material is DuPont Riston 110F; other materials may also be used(e.g., Dynachem) if necessary.

Using the photoexposure unit (Fig (18)) a photoplate is placed over the circuit, aligned to it, and clamped with a vacuum pull-down. The plate is exposed and developed in 1,1,1 trichlorethane. The spray developer (Fig (19)) consists of three stages: a spray for coarse developing, an isolated chamber for second clean-up developing, and a final deionized water rinse.

The "opened",photoresist coated,thin film circuit is now dried with clean air and examined visually. Four parameters are looked for: (1) complete coverage, (2) good clean opening of the apertures over the entire area, (3) a graduated "edge" to the aperture, and (4) the absence of blemish and other defects. A negative test result requires recycling of the circuit after a strip and peel operation. A visual check in this step is made for residual resist and for integrity of the thin film deposits. Any failure here results in a reject.

The short exposure time allows fast throughput at this stage, and therefore it does not represent a constraining step in the sequences

except insofar as alignment can be occasionally difficult. Fig (20) summarizes the process sequence at this stage.

3.3.2 Step II: Phosphor Screening Process

This step includes important material preparation and control procedures. These are therefore considered separately. The process itself will be discussed first. (See Fig (21)).

The accepted circuit plates are loaded onto a movable support that is moved back and forth with a geared drive. A phosphor/binder spray mix (see below) is prepared and a controlled spray procedure employed. A six-layer sequence is now employed with an air bake (135°C) between each step to ensure that each layer is dried. This method has been found to result in smooth, consistent, and uniform coatings. The substrate makes several automatic passes across the spray gun, which is fixed in location. All distances, angles, time of spray, etc., are fixed to ensure reproducibility. After completion of the phosphor spray, the surface is treated with a filming resin (methylmethacrylate) to ensure a smooth top electrode surface. This is accomplished with an aerosol spray of commercial "clear coat" for a controllable time, followed by a final 135°C bake.

The influence of this process on the brightness deterioration (phosphor life) is significant. Our present practice calls for rigorous drying of all equipment and materials, and the multiple bake steps ensure good dryness. Our test procedure in this process stage consists of check sample. This is the procedure now used to maintain process standards, an acceptable screen weight from this sample is the

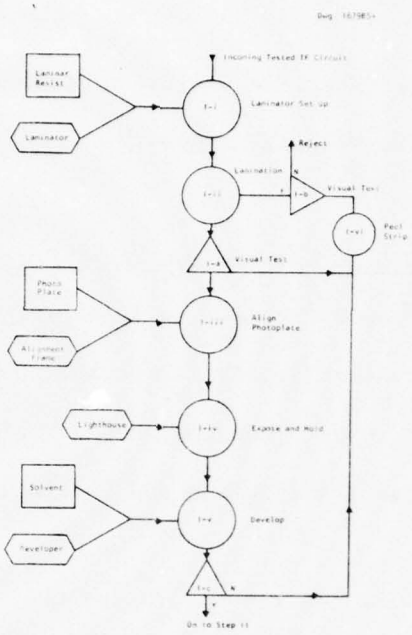


Fig (20) Summarized process sequence - Step I

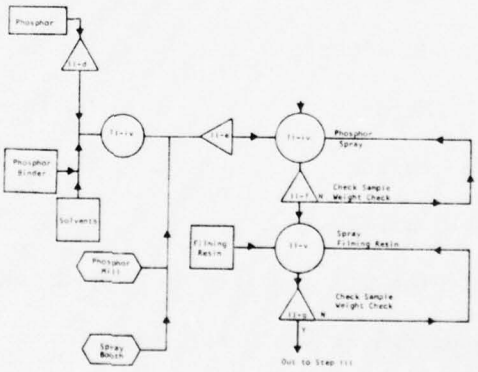


Fig (21) Phosphor screening process - Step II

go-ahead for the next step. A failure at this step is generally not irretrievable, and respraying is possible.

3.3.3 Step III. Phosphor and Spray Preparation

This portion of Step II is dependent on certain materials that are not routinely available. In particular they include the substrate glass, the phosphor itself, and the phosphor slurry. Our present practice relies on purchased glass and Westinghouse-synthesized phosphor.

The following describes in steps the synthesis of the phosphor:

(a) The ingredients

ZnS	95 mole-%
CdS	5 mole-%
Cu-acetate	1 mole-%
NH_4Br	2 mole-%
sulfur	about 2-3 grams

are thoroughly mixed.

(b) The mix is fired in capped quartz tubes surrounded by slowly flowing H_2S at 800°C for 1 hour.

(c) The pre-fired phosphor is powderized and the same amounts of NH_4Br and sulfur as above are added once again.

(d) A second firing is made in capped quartz tubes surrounded by stagnant N_2 at 600°C for 1/2 hour followed by rapid cooling to room temperature.

(e) About 30 grams (not more) of the phosphor is baked in open boats in stagnant air at 600°C for 2 hours. The hot boats are then pulled out of the furnace and rapidly quenched to room temperature by exposing phosphor and boat to a stream of cold air.

(f) The phosphor is powderized, washed in hot cyanide solution, in water, dried again, and sifted through 200 mesh.

The phosphor is now ready for us. It is a free flowing powder of particles in the 5-10 μm range. Its body color is olive-green, its luminesence under excitation by ultraviolet is yellow-green.

This batch type process can be scaled up without loss of product quality, and since the total phosphor quantity required by the display is small (∿1 g per display) and since only "good" circuits get to the stage of being sprayed, the need to convert to a continuous type process is not major.

In addition to the phosphor, a slurry for spraying is also required; this process has also been developed over several years for several programs.

The processes now formulated consist of two steps: plastic solution and phosphor spray mixture.

Plastic Solution

1. Mix cyanoethyl sucrose and cyanoethyl starch in dimethyl formanide (DMF) and acetonitrile.
2. Place the jar on a milling machine for 3 or 4 hr.
3. Add adsorbent molecular sieve to the plastic solution.
4. Filter the solution.
5. Store the plastic mixture in a tight bottle.

Phosphor Spray Mixture

1. Mix Westinghouse hypermaintenance EL phosphor power to the plastic solution.

2. Ultrasonic thin slurry for 5 min.

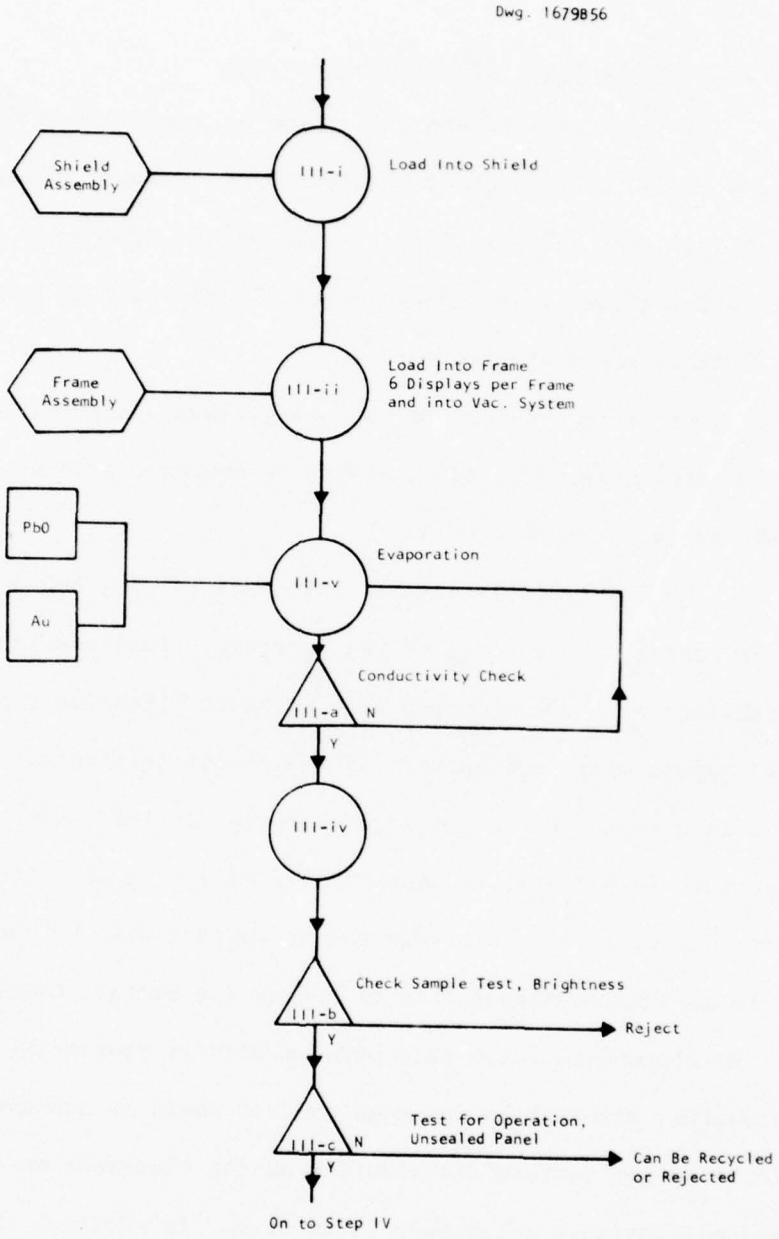
3. Start spraying. Shake slurry immediately before each layer.

The high dielectric binders have shown considerable variability in the past depending on the source (Eastman Kodak, or Techwest) but in general the process was reliable.

3.3.4 Step IV: Top Electrode Evaporation

Phosphored displays from Step II are now electroded following our normal procedures (see Fig (22)): with a substrate-to-boat distance of 18 in., PbO is evaporated first, followed by the evaporation of Au. The evaporation is monitored by measuring the resistance of the deposited layer on a microscope slide or by using a quartz crystal thickness monitor. The evaporation is stopped when this resistance on the microscope slide is about 50 ohms/square. An edge connector shield is placed around the display periphery that keeps the logic contacts clear but connects to the top electrode.

The small check sample that follows the display through phosphoring is electroded simultaneously to the display. It is then used in the approval test at this step.



Step III Top Electrode Deposition

Fig (22) Top electrode process - Step III

3.3.5 Second-Level Electroding Process

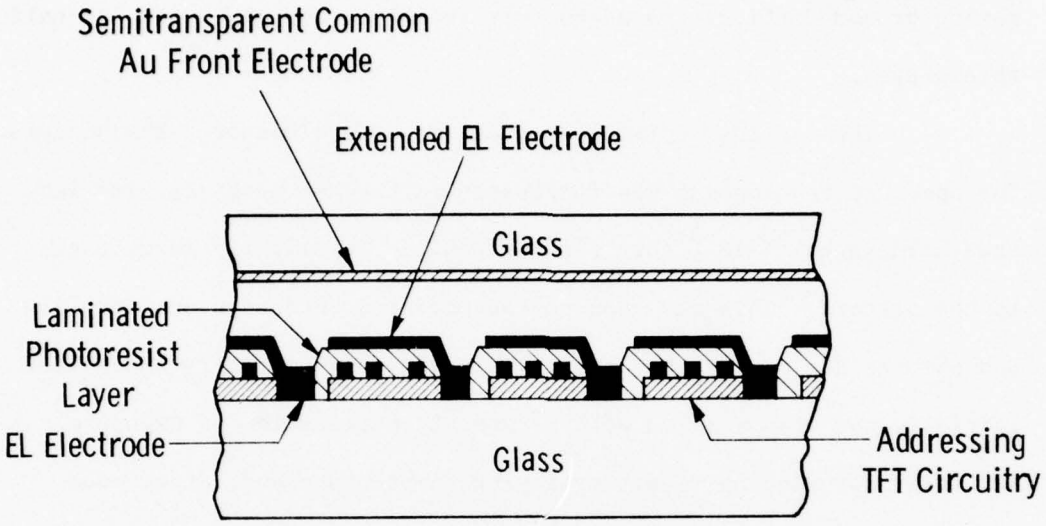
In order to increase the active or percent "lit" area of the display a second level process was developed. This involves extension of the EL pad over the thin film circuit area with electrical isolation preserved using the laminar photoresist already used in the process. Fig (23) illustrates the concept.

Our first problem was obtaining clean apertures in the contact area. Optimum methods based on Riston recommended procedures were used and largely solved this problem.

The major difficulty met with was forming and maintaining reliable contact at the edge of the aperture. This problem results from the inability of the evaporated thin films to effectively penetrate around corners with continuity. If the resist is properly developed, i.e. it is ensured that no residual material is left, then the edge of the aperture is overhung as shown in Fig (24). In depositing the electrode it will fail to bridge and no contact will be made. If the aperture is underdeveloped then of course the overall contact will be poor. An attempt to solve this problem with rf sputtering was unsuccessful; although better edge contact could be achieved it was difficult to get uniform distribution of top electrode metallization (aluminum) over this relatively large area. In addition the pattern sharpness was not adequate, good pad isolation being of course still needed.

Evaporation at an acute angle was attempted, i.e. the treated TF circuit is placed at a sharp angle to the aluminum evaporation source.

Dwg. 6358A19



Cross-sectional view of an EL panel with extended electrodes

Fig (23) Second level concept for increased lit area

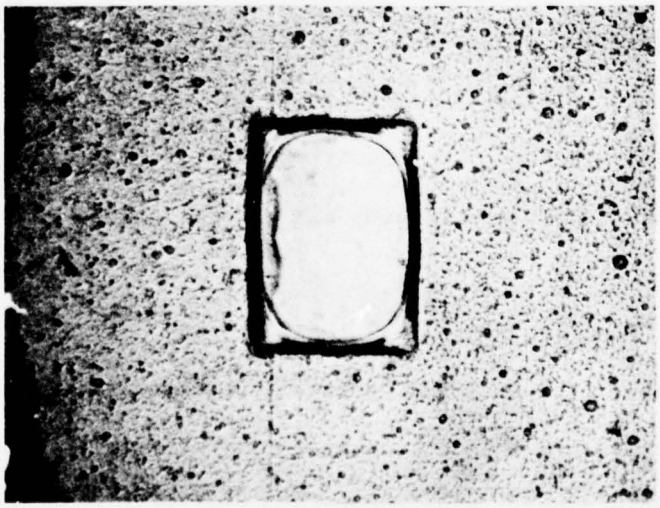


Fig (24) Overhung aperture in second level process

RM-74174

The substrate is then turned 180° to pick up the other side. This method proved difficult to adequately implement and gave very non-uniform thicknesses.

The eventual optimal approach was the simplest. The phototool for aperture development was fabricated in the X-Y mask jig with less than hard vacuum ($\sim 10^{-5}$ torr), this resulted in slightly fuzzy edges to the pattern. This was then contact printed onto high quality film and used as the master phototool. This was only partially successful initially but when combined with a careful optimization of exposure intensity, developing time, developing temperature and, after much experimentation regarding holding times on the resist, resulted in near 100% first to second level contact. Fig (25) shows the resulting electroded apertures at various magnification levels. Fig (26) shows a close up of some operational elements. Subjective examination of the resulting displays shows that the increased lit area (now ~75% of total available elemental area) has a dramatic effect towards improving the overall legibility and area brightness of the device. After optimization the process worked well and reliably.

3.3.6 Step IV: Final Seal and Packaging

The final seal and packaging process used in this program is based on methods that have been used on similar electroluminescent phosphor radiographic image converters that were produced for several years by the Westinghouse Industrial and Government Tube Division. This process is best performed on an individual basis since it is not readily

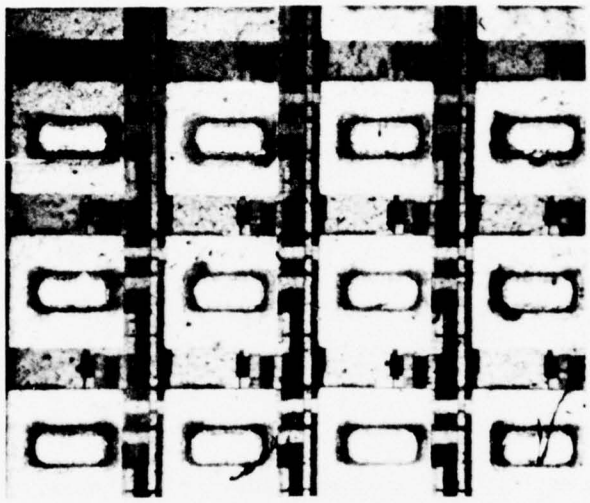


Fig (25) Actual second-level electrode pads

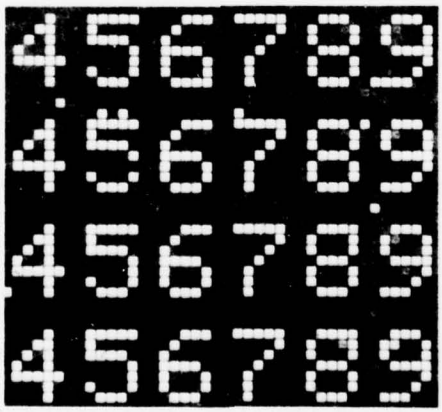


Fig (26) Second level operation

automatable and requires a relatively high degree of labor input. Two factors alleviate this potentially restricting stage: First, only displays that pass the test sequences and the initial "nonsealed" operational test are sealed. Second, the process has proven to be reliable and routine in most instances.

The sequence of the process is given in Fig (27). The tested display is sprayed with a "clear coat" resin, and the edges are shielded. The epoxy is poured over the panel and the top plate placed over it and compressed in place. Excess material is wiped off and the panel cured. The contacts are then chemically cleaned and solder dipped to improve the contact reliability for spring insertion contacts or to provide a bond for solder contacts. The display is now ready for final test. Fig (28) shows a complete, sealed display.

3.4 Summary and Fabrication Yield Analysis

Through careful control of the process, it has been shown that 6 x 6 inch 20 lpi and 30 lpi displays of near perfection can be fabricated.

No major breakthroughs have been required in the creation of near perfection in these matrices; indeed the designs and processes are similar to those reported in the first quarterly report.

The diligent application of good operational practices was the key. This is important, we believe, because it ensures that a production process, when such practice becomes standardized, will be a viable commercial operation.

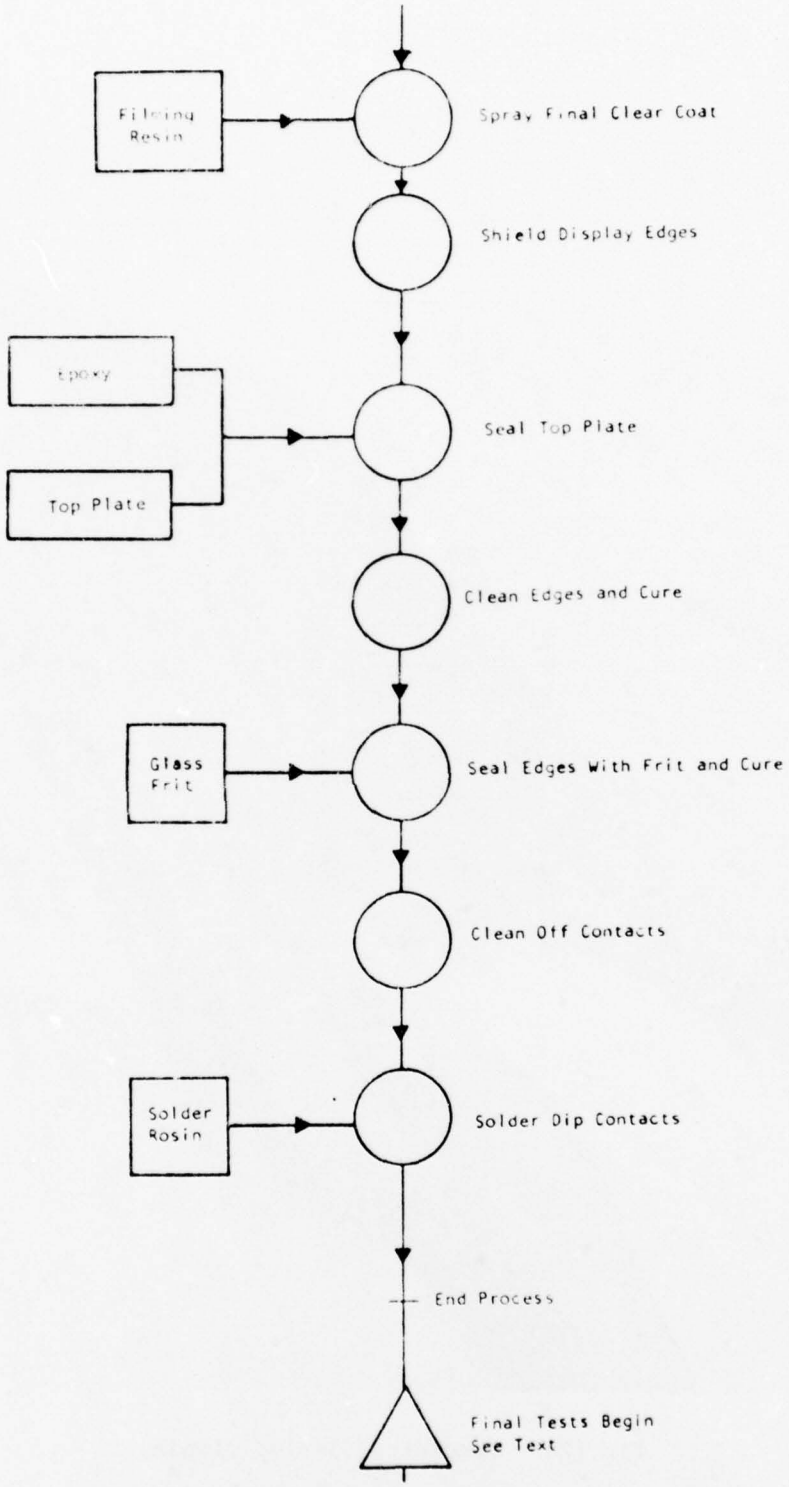


Fig (27) Final panel seal - Step IV

Fig (28) Completed, sealed display

3.4.1 The TFT Matrix Fabrication Process

An examination of production records of about 40 "starts" on the 20 lpi and 30 lpi circuits revealed that there are three categories of aborted or non successful circuit results. The analysis is as follows:

Category I - Human Error

1. Misreading and wrong jig number insertion.
2. Forgetting to raise or lower the substrate.
3. Incorrect programming of the digital controller.
4. Wrong material selection in the hearths.
5. Breakage and mask handling problems.
6. Poor control in substrate and mask cleaning.
7. Others.

Category II - System Problems

8. Evaporator malfunction (mostly e-gun).
9. Poor mask alignment initially.
10. Thermal distortion in the mask jig.
11. Failure of the jig to sustain mask reference settings.
12. Defective masks.
13. Other, as yet not identified, pattern problems arising from the mask/jig assembly.
14. Magnetic pull-up failure.
15. Cable failure.
16. Crystal monitor shifts.
17. Anneal oven failure.
18. Poor vacuum develops in a run.
19. Early mask peeling.

Category III - True Process Variability

This is hard to define but it refers to situations where everything goes correctly and the pattern is correct but the TF circuit is still not usable. The basic failure modes are:

20. TFTs not in spec. despite correct process.
21. Shorting between crossover despite good insulator and cleaning processes.
22. Intracell shorting, in the TFTs or the capacitor despite good insulator and mask/pattern definition.
23. Devices in specification but exceptionally trappy and drift prone.

If all three categories are satisfactory then the circuit has to be processed through the subsequent stages.

Table 3-3 summarizes the analysis of these circuit fabrication steps.

Table 3-3

RESULTS: PROBLEM ANALYSIS - 40 "starts"

AREA	PERCENT IN THIS CLASS	MOST SIGNIFICANT PROBLEM STEPS*
Category I Scrap (Human Error)	20%	1, 6, 2, 5
Category II Scrap (System Failure)	40%	9, 11, 19, 10, 13
Category III Scrap (Basic Failure)	10%	21, 22, 20, 23
Subsequent Process Scrap	25%	mostly photoresist see next section
Good Display	5%	*in order of most significant per category

This analysis, albeit incomplete, is encouraging since in a production environment a large part of human error will be eliminated with automation. Such minicomputer controlled processes are being developed for TF processes and the entire running of the system is readily automated. This will also help in Category II, the system failures. However the largest failure mode segment is unquestionably related to the inability of our present mask movement jig to accurately reflect the input numbers through a long sequence of depositions and waiting periods. A related problem is poor mask alignment due largely to the relatively crude method of establishing the initial alignment. These factors will be much less important in production since it is likely we would use "dedicated" individual level masks rather than the movable jig. This would minimize several of the problems and, in particular, eliminates 9, 11, 19 and probably most of 13. Further a

greater degree of reliability can be expected in production equipment if properly designed and debugged. The lab equipment is in almost continuous modification with consequent loss of immediate reliability.

3.4.2 The Display Assembly Process

A detailed analysis of fabrication yield for the packaging process was developed from the laboratory program. Of course the major source of incomplete "starts" is the TFT circuit plate. However, about 25% of the scrap of the overall R&D process is due to the subsequent processing of the circuit plate. This has been analyzed and the overall results are shown in Table 3-4. These data apply to the single level process only.

Despite this extensive list of trouble spots, which are common to all complex processes, it is encouraging that hard and fast identification of most of the variables has been achieved. These variables are for the most part correctable given time, effort, standardization, and some training. Further, the as yet unassignable problems are probably due to poor observation and are in fact due to human error not yet detectable. These are all typical variables that a production process can clarify and control; the degree of control already achieved is very hopeful in terms of anticipated eventual production processes.

Table 3-4

Yield Analysis for Packaging Process

Class	Percent of Total Attributable	Major Items in Order of Importance
Category I Human Error	55	8, 4, 9, 11, 14, 16
Category II Process malfunction	35	17, 20, 23, 24
Category III "True" irreproducibility	10	27, 29

Category I: Human Error

1. Edge connector mask not aligned properly.
2. Incorrect exposure time used in photoresist.
3. Incorrect developing time in photoresist.
4. Incorrect alignment of phototool in photoresist.
5. Phosphor spray mix formulated incorrectly.
6. Phosphor spray timing incorrect.
7. Filming spray timing incorrect.
8. Inadequate drying time-temperature of phosphor layer.
9. Incorrect sequence in spray/dry steps.
10. Poor shielding of edges in phosphor spray.
11. Poor shielding of edges in gold evaporation.
12. Edge wire contact not made.
13. Epoxy catalyst incorrectly measured.
14. Epoxy cure incorrectly timed.
15. Top seal plate mislocated.

16. General breakage due to mishandling.

Category II: Process Malfunction

This category is not readily classified as human error but includes those factors that are due to inadequacy in process control. It is assumed that the nominal process specification was followed in all of these.

17. Poor "clean out" of photoresist apertures.
18. Adhesion failure of photoresist in subsequent processes.
19. Minor defect in photoresist arising from "bubbles" or other inherent defects in the material.
20. Misregistration of photoresist mask with thin film circuit electrode due to mask or pattern distortions.
21. Voltage breakdown in resist during operation due to "thinning" of the material in developing.
22. Voltage breakdown in the EL layer (too thin) arising from process control inadequacy.
23. Low brightness in the EL layer (from too thick a phosphor/film layer)
24. Poor conductivity in gold top electrode due to residual solvent in EL layer despite good dry cycle.
25. Poor conductivity in gold top electrode due to poor vacuum in evaporation process.
26. Poor EL life due to high humidity in panel seal step.

Category III: True Irreproducibility

These are the variables that are as yet not identifiable and cause unassignable problems. It is anticipated that these will eventually be reduced to Category II.

27. Lack of uniformity in operational brightness despite good TFT uniformity and subsequent process within specification.
28. Patches of unmodulatable lit phosphor in surround of "active" pads.
29. Regions of "off" elements despite positive indication in thin film circuit panel test.
30. Completely dead display despite nominally good process.

In conclusion, this analysis is optimistic in that although the overall "yield" is ∿5% the sources of the problems mostly relate to the preliminary R&D type process we use. This was known to be more error and failure prone but does allow us rapid and immediate design changes, an important constraint in lab equipment but not so relevant in production processes. The discussion in Appendix III describes the plans and progress towards a manufacturing process.

4. Results Achieved

4.1 Introduction

Three specific formats were examined in this program; 6" x 6" at 20 lpi, 6" x 6" at 30 lpi, and the so-called DMD format 3.4 x 6.6" at ∿30 lpi. In all cases the actual active display area dimensions are slightly less than the overall dimensions since a border for edge connect fingers is provided.

To illustrate the overall display quality, in particular defect quality the following figures are illustrative of the best devices fabricated, see Figs (28) through (30).

This section will now discuss the various aspects of performance, viz. measured display performance attributes including legibility; contrast; power dissipation; life and electronic input requirements. Also discussed will be the measured performance regarding environmental properties (shock, temperature etc). Finally we will discuss TFT device properties achieved especially as regards stability since this is of especial interest. The first subsection has a brief discussion of the reasons for the residual defect sources and the objective of a perfect display.

Fig (29) Operational 6" x 6" 20 lpi displays

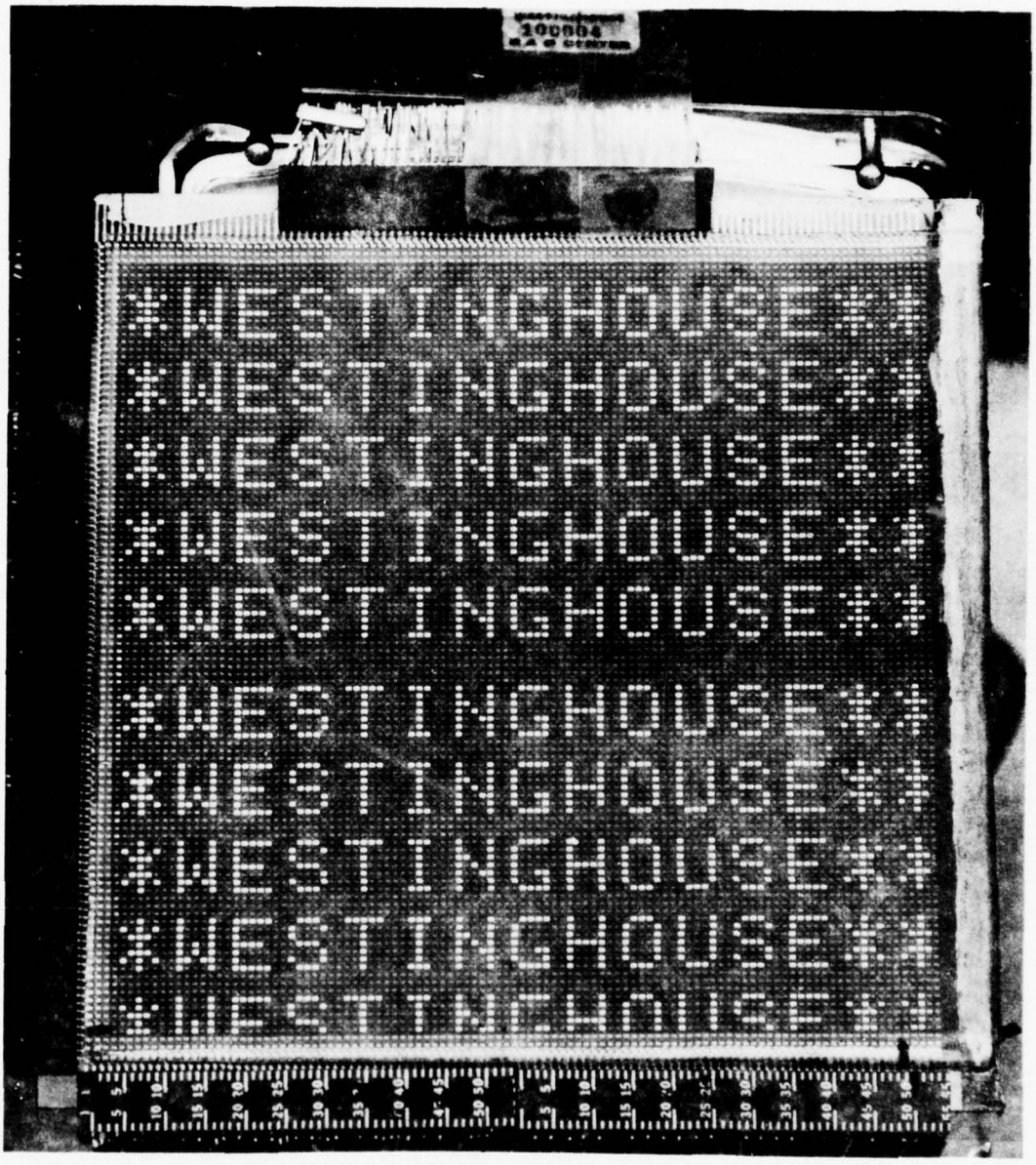


Fig (29) Operational 6" x 6" 20 lpi displays

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Fig (30) Operational 6" x 6" 30 lpi displays (2-level)

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4.2. Display Defects

As is evident from Figs (28) through (31) the display quality level achieved is already at a reasonable commercial or military standard. However residual defects remain, they include:

- o elements that are permanently on
- o elements that are permanently off
- o unconnected or broken lines that are either grounded (off) or float (on or off)
- o crossover shorts that cause crosstalk.

The on elements are caused by a variety of sources, for example:

(a) A short between the power device (T_2) gate to drain causes a series capacitance condition that lights the elements

(b) A short across the cell capacitor causes the power device gate to be pinned close to ground; the result is that the TFT is on and hence the EL cell is lit.

(c) A power device channel short permanently lights the EL element.

(d) In addition if opens occur at the T_2 gate, or T_2 drain, or T_1 drain then the result is a lit element

(e) Elements are off if, for example, T_1 gate is shorted to the drain so that the V_{bias} gate (average - 40V) pulls down the T_2 gate.

(f) Line opens or line crossover shorts are much more significant with respect to display legibility then are elemental defects. The exact condition depends on the electrical state of the line at that instant, a logic device crossover short (or T_1 gate to source) causes arbitrary

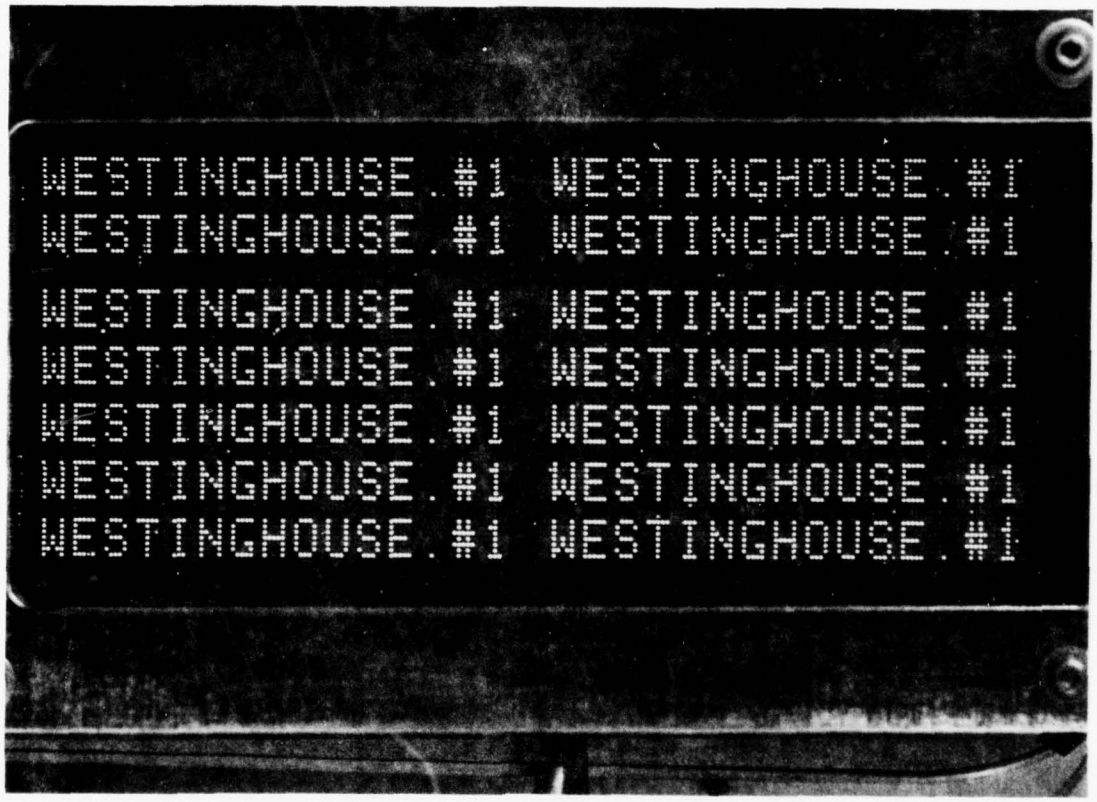

Fig (31) Operational DMD type displays

on or off unmodulatable lines, similarly a T_1 gate to ground bus bar short. An open busline will float on, picking up the ac-EL voltage; alternately if it is grounded it will be off.

The key to this discussion is that two ingredients (opens and shorts) explain virtually all the display defects. A discussion of the sources and resolutions of such defects is given in Section 3.2.4 above; as can be seen from that discussion the problems are not fundamental but relate to such factors as cleanliness, mask quality and film deposition control. When one couples these readily defined problems with the simple repair and patch techniques now being developed, then the objective of a "perfect" display appears to be attainable.

4.3 Display Properties

4.3.1. Legibility: brightness and contrast

Several factors influence legibility, which is ultimately a subjective human evaluation judgement rather than a technically defined term. It is also a controversial subject but at least some facts are incontrovertable. A certain level of brightness (i.e. luminousity) is needed as is a certain lit area per cell. A degree of contrast is required between the lit cell and the unlit cell and is also required between the lit area and the surround in a cell. Finally the level of ambient light is important when defining those parameters and the reflectance of ambient off the front is also a factor.

As regards brightness, Fig. (5) illustrates measured brightness of a cell as a function of EL drive voltage. In practice a limit is

imposed by the ability of the TFT matrix to switch the EL drive voltage and the display is limited to the 30-50 fL region. The reason for the spread lies with the variability possible with change in EL phosphor layer thickness. Thicker films are lower in brightness for a given EL drive voltage; on the other hand the thicker the film the better the life. The lower end of the range (30 fL) is preferred and this has been found to allow good legibility in room light and with filters to allow reasonable legibility in directed 4000 fc gun ambient light. Two filter systems were examined. One was a standard circularly polarized Polaroid(R) green filter which helps ambient reflection and has a certain degree of selective transmission enhancement. The other filter system is based on a black louver arrangement that selectively blocks ambient while allowing full output brightness through the louver angle This of course does reduce viewing angle but not severely. Fig (32) illustrates contrast ratio as measured with Spectra(R) spot brightness meter in an ambient of up to 10,000 fc produced by a 3200°k photographic flood lamp. The contrast is defined as:

$$C = 100 \frac{B_t - S}{B_t} \%$$

B_t is the total brightness on a lit spot

S is the scattered brightness on an unlit spot

As can be seen from that figure using the transmission filter the contrast ratio at 4000 fc is >40% at a 40 fL average brightness. This indicates satisfactory legibility under that condition, which correlates well with our subjective results.

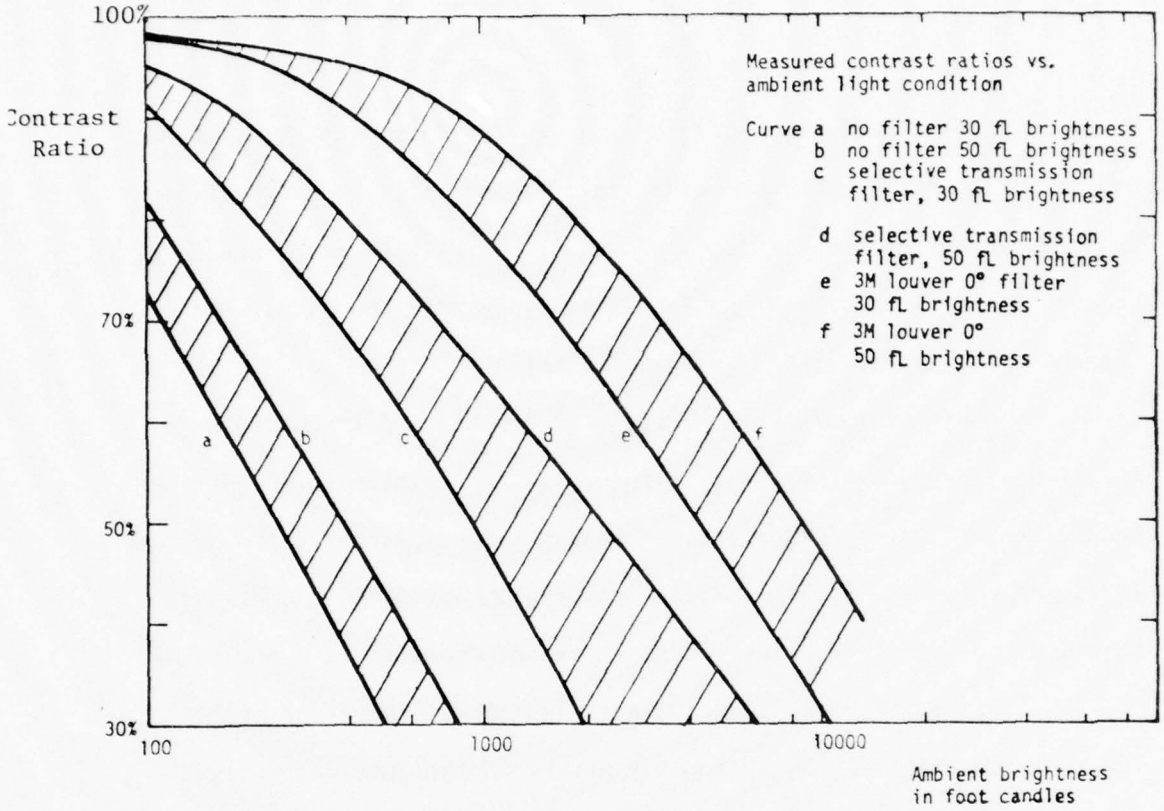

Fig (32) Display contrast as a function of ambient brightness

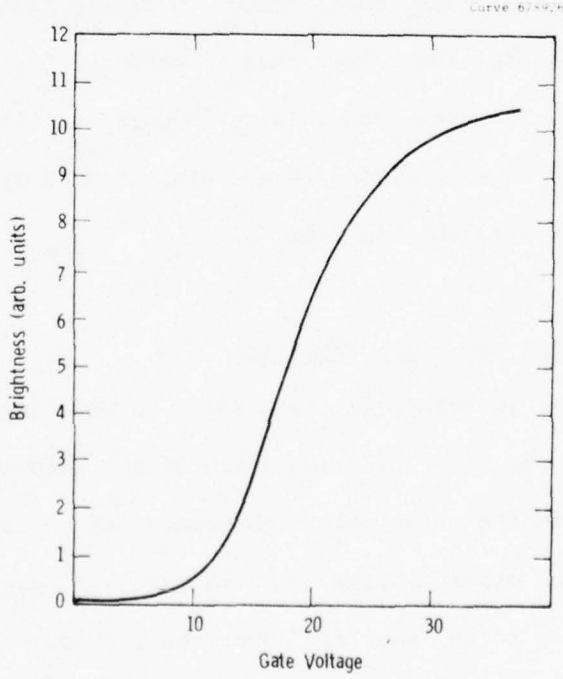

Fig (33) Contrast as a function of TFT gate bias

Addition of an evaporated black layer under the EL electrode pad (black "smoke" SiO being used) improved legibility at high ambient but reduced brightness. Further effort at black enhancement was deferred because of the much greater potential possible with the evaporated phosphor films as described in Appendix III.

Contrast [on/off in an element] can also be evaluated as a function of gate bias, Fig (33) illustrates the relationship under the conditions of 50 fc ambient on the display. The contrast ratio exceeds 100:1 and there are about 11 $\sqrt{2}$ intensity grey levels in the transfer function, an important point for video use as detailed in Appendix II.

Although these figures are reasonable it should be pointed out that the highly light reflecting nature of the phosphor and top gold electrode does cause difficulty at high ambient brightness levels especially if the ambient is "non directed" as is the case with hazy bright sunlight. Attempts have been made to make the top gold non reflecting and it is believed that this would work well if optimized. However further work in this direction was discontinued with the upsurge in results in the evaporated thin film EL.

4.3.2 Electrical input requirements

The ease of interface of the display to existing, solid state data sources is the result of the separation of the information electrical input from the relatively high voltage of the ac-EL power source. Thus, unlike other display technologies, e.g. gas plasma, where information has to be "overlaid" over the 250V or so drive voltage, the information can be provided at reasonable voltage levels,

Table 4-1 summarizes the optimum typical requirements. Two factors are important here; firstly these voltage levels do vary somewhat from display to display. Our data indicates that under semiproduction conditions (e.g. as are found in our computer controlled pilot line operation) the optimum settings are within a few volts of these levels in >75% of the good displays made. This of course excludes bad displays where errors or process problems occurred. Note also of course that whereas +10V is optimum for source positive this means that anything above that is usable as long as breakdown or accelerated drift problems don't become significant. The table lists, therefore, limit ranges as well as optimum values. Displays were successfully refreshed between 30 Hz and 250 Hz, however the 30 Hz limit is somewhat difficult to maintain over many runs; a more comfortable limit is 60 Hz. A variety of EL drive waveforms were found acceptable. Square wave when compared with sinusoidal gives higher brightness per p-p volt but does result in a small compromise in phosphor power efficiency. Triangular waveforms are also usable and are a good compromise between square wave and sinusoidal. EL phosphor drive frequency is optimal around 5 kHz but 4-10 kHz is an usable range. The effect of EL waveform frequency on phosphor properties is discussed in Section 4.5.

Table 4-1
Electrical Input Parameters

Source	positive	+10V
	negative	-20V
Gate	positive	+15V
	negative	-40V

4.3.3 Power Dissipation

In the evaluation of alphanumeric or other display panels, the value of their dissipation is of primary importance. However, the measurement of the dissipation is not too easy. Very few wattmeters can be found on the market which will measure dissipation of display panels where non-ohmic impedances and non-sinusoidal voltages with frequencies in the range of 10 kHz are encountered.

Dissipation of plastic embedded, and TFT-EL alphanumeric displays were measured with this electronic wattmeter. From the dissipation, brightness and current data the luminous efficiency and the power factor were calculated.

Figure (34) shows the brighness and efficiency data of a plastic embedded thin EL cell made of hypermaintenance phosphor. The effect of a thin SiO_2 coating on the NESA coated substrate shows up by the improvement of the efficiency. Figure (35) illustrates a summary of measured phosphor layer properties, current, power, etc. Figure (36) shows luminous efficiency as a function of various frequencies.

Measurements of complete displays of various formats, sizes and resolutions are given in Table 4-2.

In summary it is clear from Table 4-2 that we have realized our overall aim, viz, the use of the active TFT matrix has allowed us to select a display medium that has good power efficiency since we are not constrained by the need to use a matrix selection medium. The very low power dissipation of the displays is a very attractive feature.

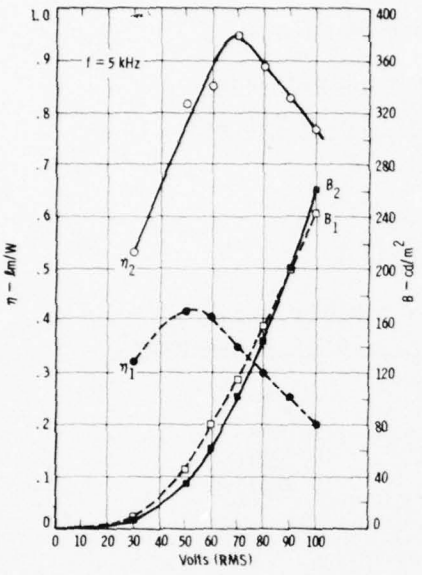

Fig (34) Brightness & Efficiency of EL cells. No. 2 with a 0.24 μm thick SiO_2 film, No. 1 without insulating film

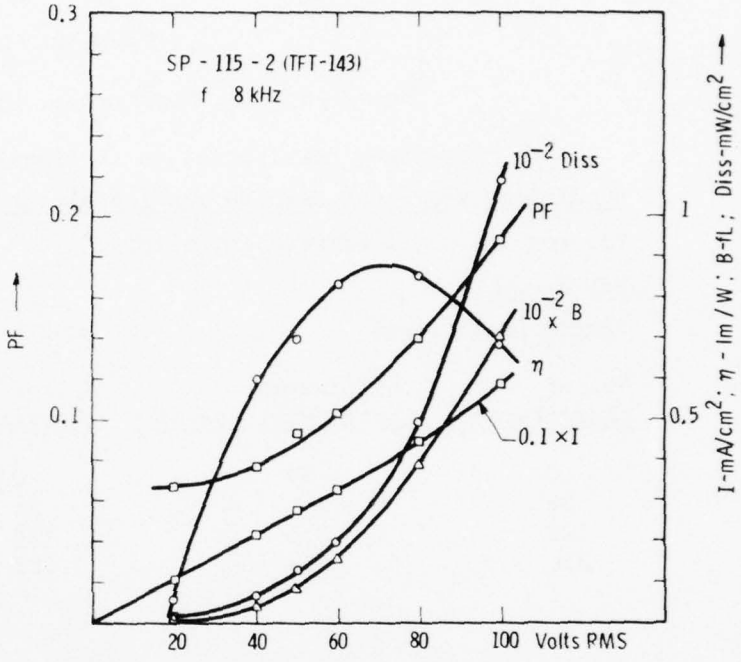

Fig (35) Summary of Phosphor Properties

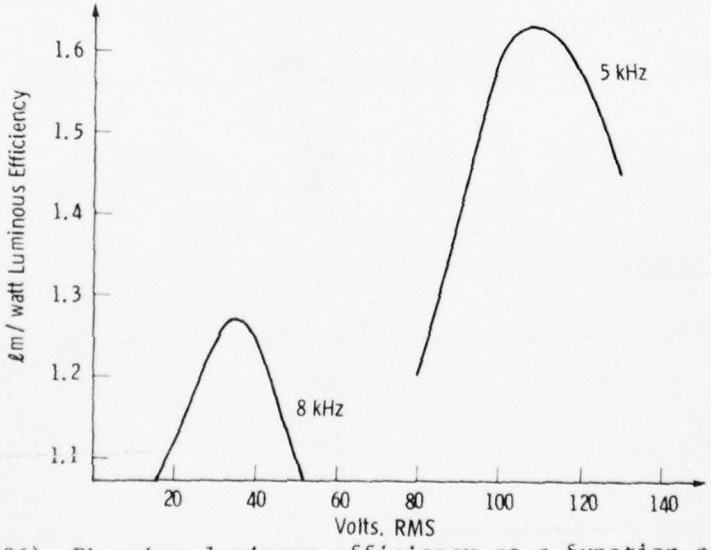

Fig (36) Phosphor luminous efficiency as a function of frequency

Table 4-2

Measured Power Dissipation in Various Displays

The power dissipation in the panels was measured under conditions where the display was legible at 2000 fc (with filter). The results obtained were as follows:

DMD FORMAT

Single level panel		Double level panel	
No. of characters*	Milliwatts total whole panel	No. of characters*	Milliwatts total whole panel
0	50	0	135
56	145	56	390
128	235	128	520
256	425	256	980

6" x 6" 20 lpi format

No. of characters	power (MW)
130	700
65	475
0	130

6" x 6" 30 lpi format

No. of characters	power (MW)
70	355
140	470
280	580
320	610

(*8 character on the display in all cases)

4.3.4 Military Environmental Properties

Although environmental testing was not a part of this program some tests were conducted. In addition from the nature of the device construction certain conclusions can be anticipated. In this section each of the prime areas relevant to Army field equipment (e.g. MIL STD 810) are briefly touched upon.

Temperature and Thermal Shock

Detailed tests on phosphor lamps made in a manner identical to the displays have indicated that no significant brightness or efficiency deterioration occurs within the range of operating temperatures +70°C to -59°C and other tests indicate that the TFT circuits remain operational in this range. The data regarding the TFT performance at elevated temperatures is given in Section 4.4.2. The phosphor brightness and dissipation vs temperature data is given in Table 4-3.

Table 4-3

	Temp$^+$	Voltage 5 kHz RMS	Current mA	Brightness fl	Diss mW	Diss mW/cm^2	Eff lm/w
(1)	25°C	80	91.3	44	2221.1	65.7	.72
(2)	-52°C	100	65.0	44	2151.8	63.8	.74
(3)	25°C	80	87.5	45	2107.6	62.4	.78
(4)	72°C	77	114.3	45	2919.1	86.4	.56
(5)	25°C	80	93.0	43	2234.5	66.1	.70

Samples of display panels have been successfully subjected to temperature shock tests where the device was repeatedly taken from +70 to -54°C in less than 5 min. The display panel samples were tested

using methods based on MIL STD 810, Method 503.1, Procedure 1. Some simplification of these tests was utilized but the tests were strongly indicative of no problems in this area.

Altitude

The display contains no voids, gas filled envelopes, or compressible areas and is a solid laminated structure. It should survive at very high altitudes.

Humidity

The construction of the display should allow the panel to operate without significant degradation after exposure to high (100% RH, 85°F) humidity.

This display is at present sealed with cured epoxy. If necessary glass hermetic edge seals could be used.

Electromagnetic Compatibility

Initial testing of the operating panel has been conducted to determine its interference (emission and susceptibility) to electrical and electronic noise. A high frequency oscillator, with probe placed across the display, was slowly scanned up to 600 kHz. No interference whatsoever was found. Repeated switching of a fluorescent starter circuit in the immediate vicinity of the device did not affect it when the house power supply driving the test exerciser was not on the same circuit loop as the lamp. Some power line "spike" effects could be

observed when on the same circuit but these were traced to the keyboard logic circuits or were not a function of the display itself. Numerous other electronic devices such as oscilloscopes and power supplies were operated within inches of the display without interference. It is well known that the field effect transistor structure is comparatively resistant to such effects relative to bipolar devices. These tests were conducted without any face plate shielding. In practice, a transparent, grounded, conductive coating on the display could be provided to enhance its resistance to electromagnetic emission and its related susceptibility.

Examination of the ability of the display not to emit radiation that could interfere with electronic equipment was briefly conducted. A radio with aerial placed near the device did show that interference does occur at certain frequencies. This appears to be associated with the scanning circuitry employed in the display drive package and transmitted by the leads to the device. Relative to the leads, the display face itself was a minor influence as far as could be determined. A conductive shield should minimize this effect. It should be noted that the low power dissipated in the TFT-EL display should be a major factor in reducing emitted radiation relative to other display technologies.

Shock and Vibration

The display panel is a rugged and shock resistant device relative to any other comparable glass-based display. The design ensures that the panel is able to survive shock experienced in military

vehicle transportation and servicing and bench handling. Our experience with a properly fabricated panel has been very favorable.

Tests based on MIL STD 810 method 516.2 Proc. 5 were successful although further tests are required. The panel is a simple laminated entity with little potential for resonance or destructive vibration modes. No problems are anticipated in this area.

4.4. TFT Performance Attributes

As was derived in Section 2.2 the use of the TFT in the modes required for circuit operation places certain specifications on them. These include certain specific initial device thresholds and gain and also required short, and long term, stability levels. In this section data relating to the operational characteristics of the devices is presented first; then follows stability data including the results of accelerated life test data performed on individual devices. Also discussed is the TFT spatial uniformity over these relatively large areas. Finally the question of TFT reproducibility is treated.

4.4.1 Device Characteristics

This topic could well encompass many volumes similar to this report, indeed several papers have been published on device characteristics as part of this contract, (see Section 7) as well as extensive documentation in the quarterly reports. This section will therefore summarize,and in addition present some newer more fundamental data.

The transconductance (g_m) of the TFTs as fabricated in this program, were not found to be constant parameters as predicted by simple theory, but were in fact functions of gate voltage. This arises since carrier mobility in the polycrystalline semiconductor films is strongly voltage dependent. Fig (37) illustrates g_m as a function of gate voltage, and Fig (38) shows measured device mobility as a function of carrier concentration and hence gate voltage.

An unusual feature of the devices is the slow "turn on" characteristic at gate voltage near the threshold. This arises from the low mobility in this range; the I_D/I_G behavior being nonlinear. It was observed that in enhancement devices mobility increases with increasing V_G but in depletion devices the mobility increases to a maximum and then decreases.

Table 2-1 illustrates the optimal device properties that were eventually standardized upon and Fig (39) shows a typical device I/V relationship. The very low leakage or "off" current is a remarkable feature; it appears that in devices with good gain it is very possible to reduce "leakage" current to close to a limit imposed by glass surface conductivity (<1 nA) - see Fig (40). Further the device is stable for long periods in this range providing the gate is reverse biased occasionally.

Another significant advance in device technology has been the achievement of a reliable 300 V_{SD} power device. The principle reason for this lies in the high quality (intrinsic and defect) Al_2O_3 gate insulator and the 5-6000 Å gate insulator thickness possible without loss of g_m with the CdSe TFTs as developed in this program.

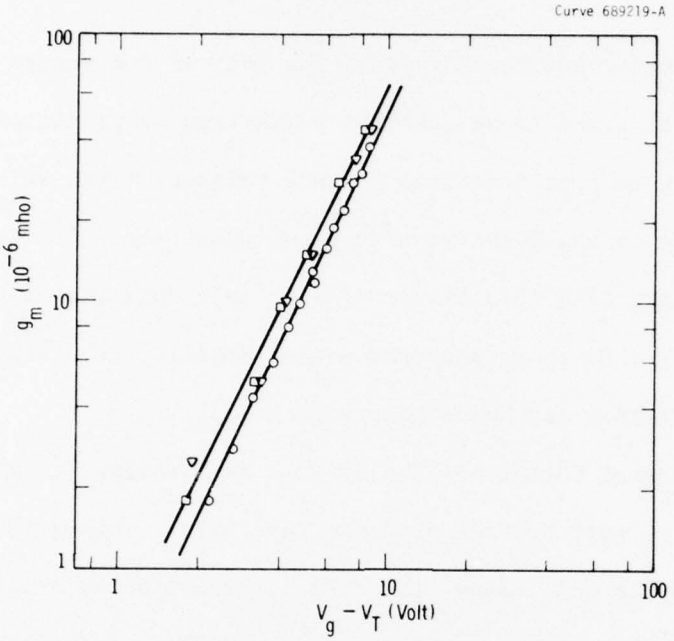

Fig (37) TFT transconductance as a function of gate voltage

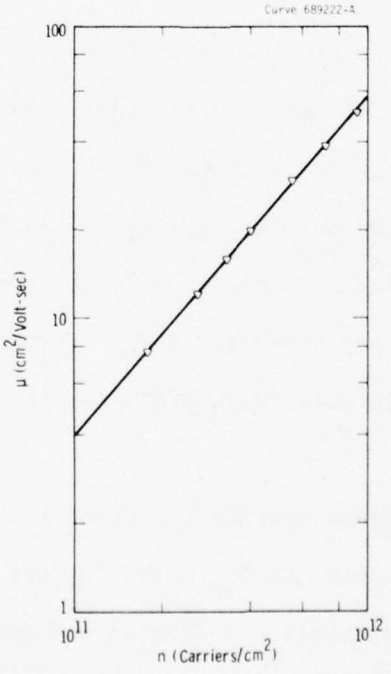

Fig (38) TFT mobility as a function of carrier concentration

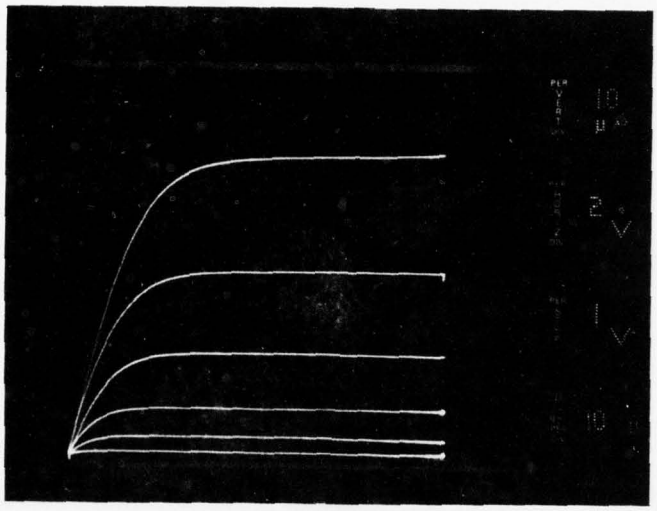

Fig (39) A typical TFT I/V relationship

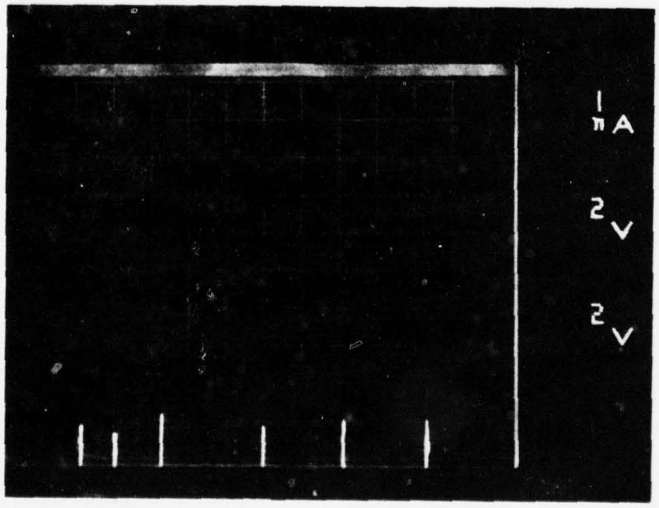

Fig (40) Ultra low leakage in a typical (T_1) TFT

4.4.2 Stability Results

Instabilities in TFTs are manifested chiefly by variations in threshold voltage and carrier mobility with time and temperature. These variations may also be voltage (or more correctly, field) dependent. In most TFT devices, the threshold voltage is the predominant field dependent instability mechanism. Both ionic and electronic processes can lead to threshold instability. However, the chief instability mechanism in TFT devices is electronic trapping, a field-dependent process whereby electrons from the conduction band in the semiconductor are transferred under positive field into the insulator where they"fall" into discrete energy states called traps. These traps can be caused either by impurities in the insulator or by defects in the lattice structure introduced during the deposition process. The lattice mismatch at the semiconductor-insulator interface can also create trap levels, often called surface states. The density of trapping states is found to vary with the type of insulator material used as well as with the deposition parameters. Post deposition annealing and surface passivation can also significantly reduce trapping.

In n-type TFT devices, electron trapping is characterized by a slow decrease in drain current with time under conditions of a constant positive dc gate bias applied to the device. The time constant for this trapping is logarithmic in nature, indicating a tunneling process between the conduction band electrons in the semiconductor and trapping centers located in the bulk of the

insulator. After all the trapping centers are filled, the drain current becomes constant. The process is reversible; that is, under negative (or zero) bias, electrons empty out of the traps and transfer back into the semiconductor.

Stability measurements performed on TFT devices were divided into two phases, short-term and long-term. Short-term stability measurements consisted simply of monitoring the volt-ampere characteristics displayed on a Tektronix 576 curve tracer for a period of 10 minutes and recording the change (if any) in the saturation transconductance g_{ms}. The transconductance of a TFT operated in saturation is given by

$$g_{ms} = \frac{Z\mu C_i}{L} (V_G - V_T)$$

and is equal to the reciprocal of the linear ON resistance of the device (c.f. eq. 7a). Changes in g_{ms} are thus indicative of changes in R_{ON}. $(I_D - V_D)$ vs V_G measurements taken at time = 0, 2, 5, and 10 minutes for each device were recorded from a number of devices selected at random; they showed an average drift in transconductance over the 10 minute interval of 0.7%.

An extensive accelerated life-test program was carried out to obtain data on the long-term stability behavior of TFT devices. Over 100,000 device-hours of reliability data have been obtained on discrete devices at temperatures ranging from 25°C to 100°C, operating under signal conditions corresponding to those used in actual display panels. 100 individual TFTs were connected in the circuit configura-

tion illustrated in Fig (41). Four groups of 25 devices each were placed in ovens at temperatures of 25°C, 50°C, 75°C, and 100°C for 1000 hours. The bias scheme, as shown in Fig (41),consisted of applying a constant dc bias to the gate electrode, while a combination of a dc bias and a 10 kHz ac signal is applied to the drain circuit; this combination being chosen to approximate actual panel operating conditions. The relays RY-1 and RY-2 form part of an automatic test sequencer apparatus which automatically scans each device under test (DUT) at selected test intervals (eg. every 1 hour, 5 hours, etc). Each DUT is scanned for 30 ms during which both RY-1 and RY-2 are closed. This momentarily "shorts" out the 10 kHz ac signal being applied to the particular TFT being scanned and biases the DUT into the "linear" region while a digital voltmeter (DVM) connected through RY-1 records the drain voltage (V_D) of the device (which is related to the drain current by $(1 - V_D)/10K$).

During this bias-temperature test a slow decrease in drain current with time was observed. This decay in drain current is a result of electronic trapping, as discussed earlier. At the end of 500 hours the biases were turned off and the recovery of the drain current was recorded for the second 500 hour period; the biases being periodically reapplied to momentarily measure the drain current.

The results of the accelerated operational life-tests are plotted in Fig (42). Shown in the upper portion of the figure are the fractional drain currents (expressed as a percentage of the initial drain current) for each of the four temperatures as a function of time under bias. Each curve represents the average result of 25 devices. In the lower portion are plotted the recovery characteristics.

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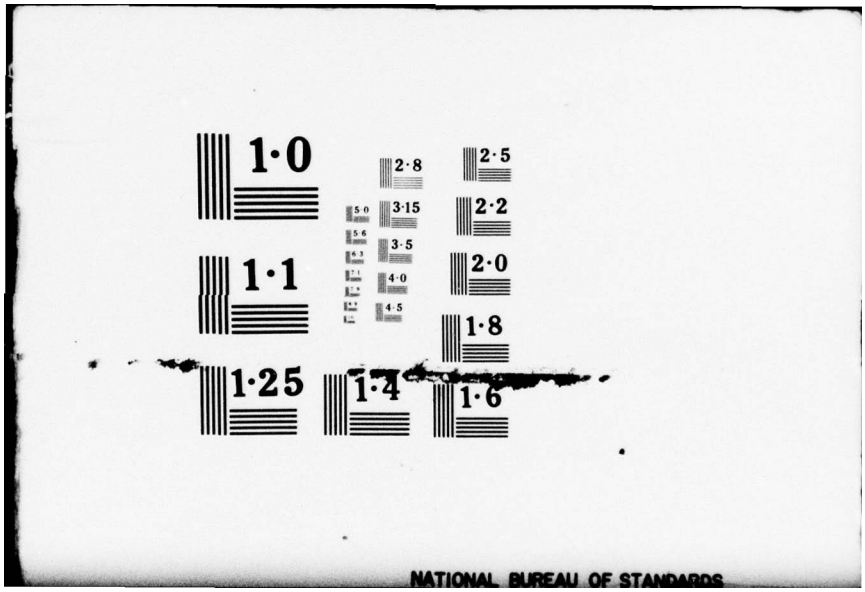
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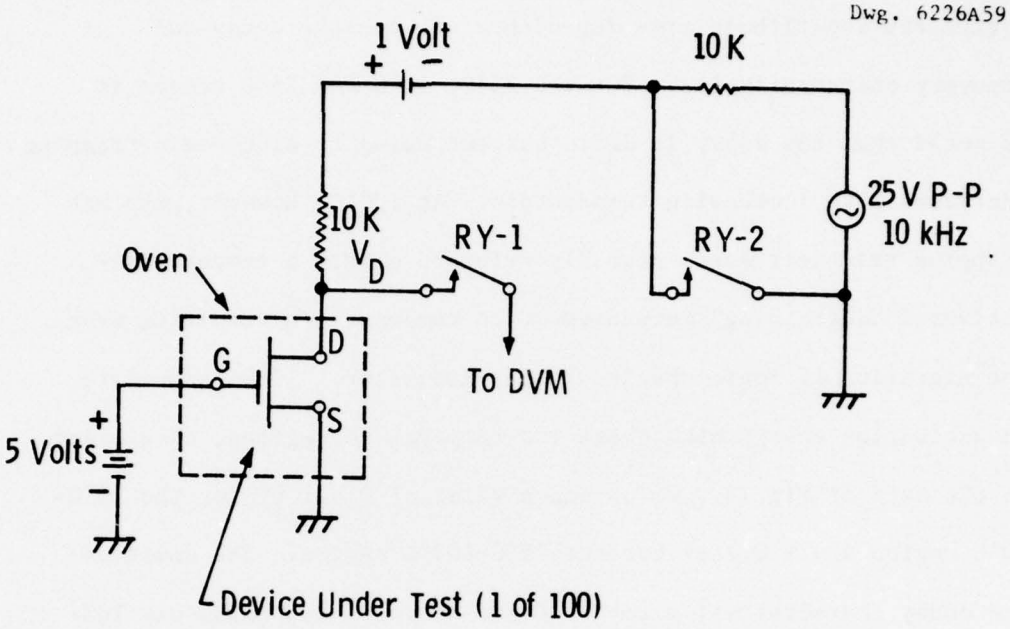

Fig (41) Test configuration

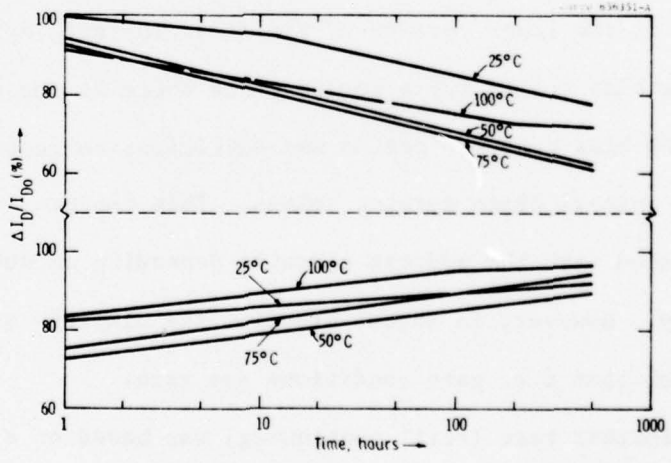

Fig (42) Accelerated long term test results

Notice the logarithmic time dependence of both the decay and recovery characteristics. For the 25°C, 50°C and 75°C ranges it is noted that the decay in drain current owing to electronic trapping increases with increasing temperature. At 100°C, however, the net trapping rate decreases, probably owing to either a temperature-activated "detrapping" mechanism or to compensation resulting from the migration of ionic species in the insulator. If we associate an activation energy with these two temperature regions, then based on the data of Fig (42),we obtain a value of 0.8-1 eV for the 25°C-50°C region and $\sim$ 0.7 eV for the 75°C-100°C region. The slope of the decay characteristics for 75°C and below is approximately 10%/decade in time and for 100°C it is approximately 7%/decade. A "half-life" based upon extrapolation of these values to a 50% decay is roughly 12 years.

It is to be noted, however, that the trapping process is reversible, as evidenced by the recovery characteristics illustrated in the lower portion of Fig (42). In fact, application of a reverse bias (-5 V) for a period of 24 hours at the end of the 500 hour zero-bias recovery period was sufficient to restore the full 100% of the initial drain current values. This feature can of course be incorporated into the address circuits depending on duty cycle etc., if necessary. However, in actual practice the displays are operated in modes such that d.c. gate conditions are rare.

A further test (still continuing) was based on a free running astable multivibrator consisting of two astable TFT switches, two TFT current source loads and two TFT output devices driving on LED.

Further details of this test are given in several of the quarterly reports; the result was as follows:

Prior to the start of the test, curve tracer I-V characteristics were obtained on device T_1. The circuit was then started and left to run continuously. The LED flashes at roughly a 1 Hz rate, and periodic data was obtained simply by measuring (with a stopwatch) the time required to generate 100 pulses. The data are shown in Fig (43). After 30,000 hr of operation, I-V characteristics were again taken on T_1, which were very nearly identical to the original set except for a slight shrinking due to a small shift in threshold voltage (approximately 0.4V) as a result of slow electronic trapping. There is no evidence of fast trapping as indicated by the equivalence of pulsed-mode characteristics and dc characteristics.

The change in the pulse period after 30,000 hr of continuous operation was 16% and can be attributed to the shift in V_T. This change in V_T with time is essentially logarithmic, so we would expect another 16% shift after 200,000 hr (25 years).

4.4.3 Uniformity and Reproducibility

The spatial uniformity of device (TFT) thresholds is important to ensure uniform operation, of course as was derived in Section 2.2.3 there is a wide latitude in typical alphanumeric operation where the matrix is essentially run in saturation. It is important however that gross variation does not occur and in fact if the goal of an integrated "internally scanned" display is to be achieved then the achievement of good device uniformity becomes much more critical.

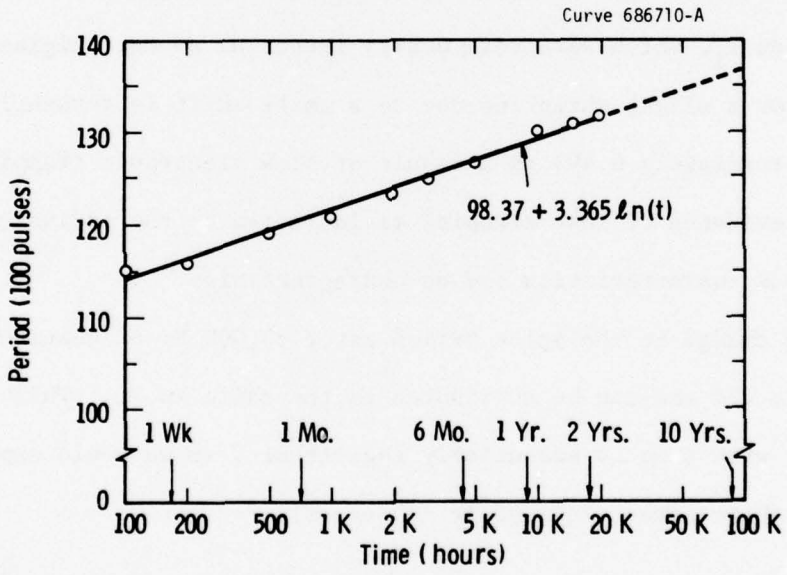

Fig (43) Multivibrator test results

Much data has been presented in the quarterly reports that summarizes, in cumulative histogram form such parameters as "off" (leakage current) at fixed V_{GS} values and ON resistances. This data will not be reiterated here except to say that the data were very encouraging with a virtual 100% acceptance over 6" x 6" areas.

More recent data has been acquired over the 6" x 3" ("DMD") displays; this data was collected with the computer interfaced automatic "Electoglas" wafer probes. Table 4-5 summarizes the results which confirms the earlier data. It appears that provided mask (and hence pattern) geometries are satisfactory, and provided that no dimples or waviness in the masks is present and hence pattern sharpness is good, then uniformity of device threshold is better than $\pm$ 10%. The grey-level video imagery shown in Fig (48) of Appendix II is direct proof of device threshold uniformity.

Reproducibility is a difficult question to adequately treat in the realm of a research contract since of necessity process parameters change as the program evolves. Recent results on the related Manufacturing Methods Contract (DAAB07-76-C-0027) where device recipes are held constant, are more relevant. Although the bulk of this data is reported in the quarterly reports on that contract the data indicates that, for example, out of ten sequential runs (7/26 to 8/22) seven had TFT device thresholds within 10% of each other and that of the remaining three one was incorrectly doped and the other two had poor source-drain pattern definition. That data is furthermore typical and not especially selected. The message is that if the process is held constant and no

Table 4-4

TFT Thresholds as a Function of Location

Location x	location y	V_{T_1}	V_{T_2}
10	13	1.1	0.6
10	15	1.0	0.5
11	17	1.0	0.6
10	14	1.1	0.5
11	16	1.2	0.4
10	68	1.3	0.5
9	70	1.2	0.5
8	71	1.2	0.5
10	70	1.3	0.4
9	71	1.1	0.5
109	38	1.3	0.4
111	37	1.5	0.6
110	38	1.2	0.3
111	38	1.3	0.5
112	38	1.1	0.5
219	70	1.1	0.4
219	71	1.1	0.4
222	68	1.3	0.3
220	70	1.2	0.5
220	71	1.4	0.6
217	12	1.3	0.6
217	13	1.4	0.5
218	13	1.2	0.3
219	12	1.1	0.3
219	12	1.3	0.4

untoward events occur then the TFT is a reproducible component. The data on that contract is further indicative in that a check of 5 early circuits (made in May 1977) compared to 5 later circuits (made in August 1977) showed that the average device threshold was within a fraction of a volt between the two groups.

4.5 Hypermaintenance "EL" Phosphor Life

Developments in the phosphor area confirmed that we have a phosphor capable of extremely long life (~7,000 hrs, 5 kHz, L_o = 30 fl for example). See Fig (44). It has also allowed us to answer the question does the phosphor actually deteriorate to a finite level or is it a very long life material that will nevertheless slowly lose brightness.

After considerable work under most careful conditions we now can define the deterioration behavior of very long living phosphors operated under constant conditions. In particular, asymptotic approach of L/L_o towards a finite level does not seem to occur. All phosphors, including very long-living ones, appear to approach zero after sufficiently long operation times.

We observed empirically that the shapes of the deterioration curves of most or all phosphors operated under "constant conditions" follow closely the relationship

$$\frac{L}{L_o} = \frac{1}{1 + (t/\tau)^n} , \qquad (1)$$

The value of the index, n, generally is between unity for short-living phosphors and 1/2 for long-living phosphors. A convenient fit of

experimental data to this equation is obtained by plotting the quantity $(L_o/L - 1)$ as a function of the time, t, both in logarithmic calibrations. This plot yields a straight line of the slope, n, and an intersection with the ordinate $(L_o/L - 1) = 1$ at the half-life, τ as in Fig (44).

Equation (1) can be, and has been, used to determine half-lifes of 10^4 hours and longer with actual test times only a fraction of τ.

Equation (1) is observed to provide a good fit to experimental data in all cases of constant operating conditions. This includes constant humidity. Fairly strong deviations from (1) may occur if constant humidity is not maintained during the life of the EL cell.

Although phosphor life is very good relative to commercially available ac-powder EL we still do not regard it as a final answer. Some difficulties in batch to batch variation caused problems and the life is still marginal for many applications.

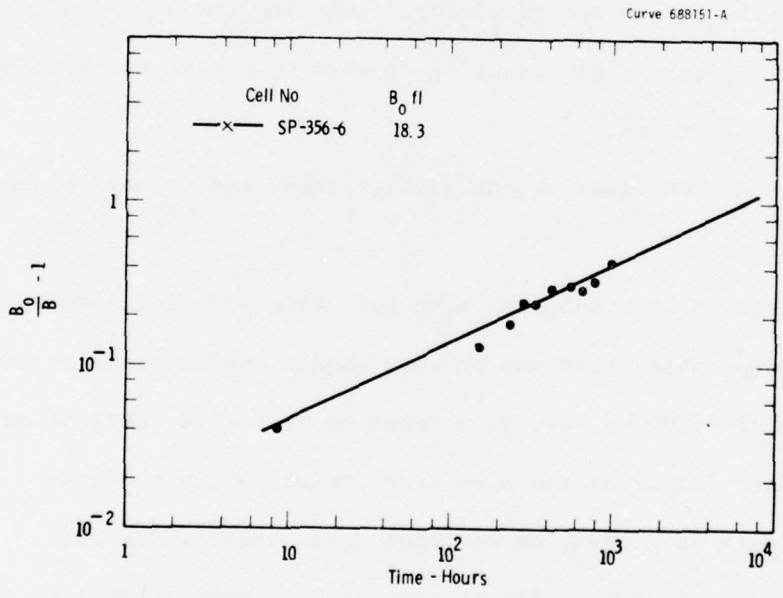

Fig (44) EL phosphor deterioration

4.6 Considerations Regarding Display Life

The factors raised by life requirements can be divided into three principal areas.

1. Brightness deterioration that will occur with operation.

2. Defects that could occur, elements or lines turning on or off and not being controllable. These could arise because of shorts or opens in the circuit.

3. Changes in the TFT properties with operation that could cause the elements to drift out of specification. This applies to the circuit plate somewhat but is more significant if we wish to pursue integrated peripheral scanning circuits.

We are confident that we can satisfy these conditions for the following reasons.

The change in EL brightness with operating life is known and definable under comparable drive and process conditions to those required here. Half lives of >5000 hr have been observed with this fabrication method, the phosphor following the slow decay relationship shown in Fig. (44). This figure is a revision of prior data[+] where a somewhat longer half life was indicated. Recent results have shown that life is strongly dependent on the method of forming the EL layer. Using a brush type approach to phosphor deposition results in a higher phosphor/binder ratio. The result is that the embedded phosphor layer has somewhat longer life than if a high binder content is present.

[+]Quarterly Report #4.

The method now used to fabricate displays (spray) results in a higher binder ratio in the eventual layer. We have discovered, therefore, that a more realistic figure for a half-life for phosphor layers prepared in the same fashion as the display is ∿6,000 hr (see Fig. (44).

It is possible to still meet, with adequate leeway, good operational life times. Using the relationship of Fig (44) and the phosphor voltage/brightness relationship, it is possible to convert a 1000 hr requirement (say) into drive voltage. We have determined that 40 fL is more than sufficient to meet 4000 fc legibility. To be able to achieve this after say 1000 hr requires that the matrix circuit be capable of handling a drive voltage equivalent to L_1, where L_1 is derived from the value of $(L_1/L_0 - 1)$. When t = 1000 hr in Fig (44) this is ∿0.40. Therefore $L_1/L_0 = 1.40$ and since $L_0 = 40$ fL, then $L_1 = 56$ fL and the required voltage drive condition is ∿90 V_{rms}. This is only marginally above the initial drive requirement of 80 V_{rms} and is well within the capability of the matrix and TFTs. This surprisingly small increase in the maximum voltage rating comes about because of the superlinear brightness/voltage relationship inherent in EL phosphor.

The question of TFT matrix "life" is well documented and reference is made[+] to previous publications on this topic. Two major factors are important: the appearance of defects (related to matrix shorting) and device drift. Two classes of defects are present in the display -- initial defects and those that appear during life. The former are counted as scrap and are not, therefore, under consideration.

[+] E. W. Greeneich and F. C. Luo publication, Section 7, p. 101.

The latter we have found come under two categories: Those which appear in the first few hours of operation due to poor quality crossovers or devices and those which appear during regular operation. Our experience is that the vast majority of defects appear during the first few hours of life. After this it is relatively rare to observe a defect appearing if the voltage used in the initial burn-in is not exceeded. This phenomenon, called "infant mortality," is common to all integrated circuitry. Based on this, we conduct a 20-hr burn-in at the maximum voltage rating after each display is fabricated. A failure here is considered part of fabrication yield, not life. (The question of initial "as fabricated" defects is discussed in Section 4-2 above).

Transistor threshold drift is a phenomenon that does occur, as indeed it occurs with all silicon MOSFET transistors. With regard to the matrix transistors, it is of relatively little significance, as has been discussed previously. The effect of drift on alphanumeric or other non-gray level displays is minimal since the devices are operating in a saturation mode. However, this is not the case for the peripheral scanning circuits. A detailed discussion of our results on drift, that indicate at least 20,000 hr of operational hours, is given in Section 4.4.2.

It is clear, therefore, that the technology can satisfy a significant life requirement. To be sure, we cannot at this stage point to extensive life data on existing displays. Such experiments are being set up now as part of the present MM&TE program.[+]

[+]USA ECOM Contract DAAB06-76-C-0027

In an initial test a 600 hrs life program was set up and run. The entire panel was exercised (every element), the gates were scanned and the sources held at constant voltage. The EL voltage was set at a value to give 2000 fc legibility. The panel was set at 50 mins ON 10 mins OFF. Bias settings, defect counts, brightness and power dissipation were measured before and after the test. The brightness results are shown in the attached Fig (45). Initial dissipated power - (all elements on) was 853 MW. The final dissipated power - (all elements on) was 980 MW. The optimal bias settings were:

Optimal bias settings	Initial	Final
S+	+12.5	+15.0
S-	-15.0	-20.0
G+	+10.0	+12.5
G-	-50.0	-50.0

No ON elements turned off and only ∿2 off elements turned on. A few (7) new shorts appeared but these were minor.

This test, although incomplete and brief, is sufficiently encouraging that no major life problems are excepted when the display moves into production.

Curve 691588-A

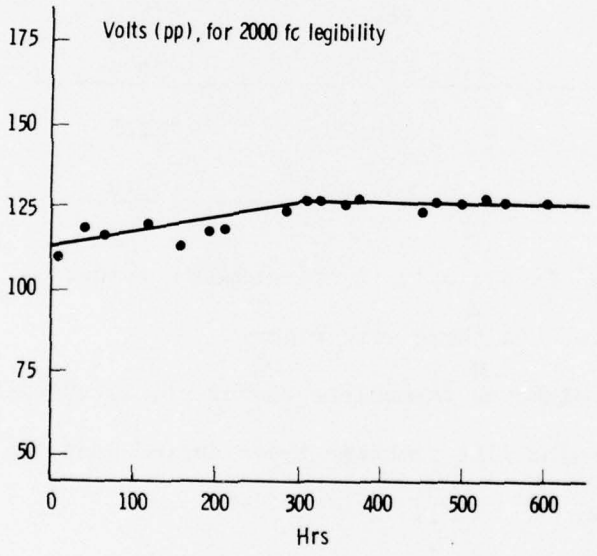

Fig (45) 600 hr constant brightness-life test

5. Conclusions

The overall conclusion from the program is both simple and clear; the concept of a TFT assisting array integral with an electroluminescent dot matrix is realizable and results in viable solid state flat panel displays of great future utility to the US Army.

The major attributes of that overall conclusion are:

(i) Large matrices of TFTs and thin film capacitors can be fabricated by relatively simple methods with minimal defects.

(ii) The TFTs are sufficiently stable,* both in long and short term aspects for militarily usable displays.

(iii) The TFTs can be made with a consistent 300V switch capability.

(iv) Low enough "turn off" currents in the devices are achievable so that frame period elemental storage is viable.

(v) The gain-bandwidth limitation on these CdSe TFTs is such that no speed related problems are evident and fast refresh real time imagery, and peripheral address scan circuits made from the same devices, are possible.

(vi) The display of grey level imagery is possible with good uniformity through source voltage modulation.

(vii) The "hypermaintenance" EL phosphor is a viable medium for solid state display; its power efficiency is excellent, brightness and life reasonably good.

(viii) That the TFT matrix can be simply isolated from the ac-EL drive voltage.

(ix) The TFT approach offers a complete solution to the problem of multi-element dot matrix addressing and the resulting displays have major performance advantages over all competing devices.

*A minor drift problem, observed in the OFF condition, has recently been corrected.

6. Contributing Personnel and Acknowledgements

During the course of this contract the following personnel have made direct contributions to the effort:

Engineering

Dr. T. P. Brody, Management
Dr. D. H. Davies, Management
Dr. F. C. Luo, TF Circuits, Riston and overall direct process control
Dr. W. Lehmann, phosphor
Dr. Z. P. Szepesi, phosphor processing
Mr. J. A. Asars, electrical design
Dr. E. W. Greeneich, electrical test and devices
Mr. R. E. Stapleton, TFT devices
Mr. A. J. Simon, contacts
Dr. H. Y. Wey, TF circuit fabrication
Mr. P. R. Malmberg, electronic analysis

Technicians

Mr. W. S. Escott
Mr. W. A. Hester
Mr. D. W. Yanda
Mr. D. Leksell
Mr. F. S. Youngk
Mr. D. Nebel
Mr. H. Dorman
Mr. G. J. Machiko

Especially tribute should be made to Dr. Luo who carried the bulk of the prime engineering process development. In addition we wish to express sincere and most geniune thanks to Dr. Elliot Schlam, Dr. Irv Reingold and Mr. Bob Miller at USAECOM for supportive monitoring courageous back-up and creative inputs.

7. Publications, Reports, Conferences and Lectures

Several papers were published during the course of the program that included data in whole or part derived from the contracted effort. Acknowledgement was made to the US Army (ECOM) in all these listed papers.

"Large Scale Integration for Display Screens", Presented at the 1975 Chicago Spring Conference on Broadcast and Television Receivers. Published in IEEE Trans. CE-21, 260 (1975). T. P. Brody.

"A 6 x 6 inch, 20 lpi Electroluminescent Display Panel" IEEE/SID 1975 Conf. on Display Systems, T. P. Brody, F. C. Luo, Z. P. Szepesi, D. H. Davies. Also published in IEEE trans. ED-22, 739 1975.

"Integrated Electrooptic Displays", p. 303, in "Non-Emissive Electro-optic Displays", ed. A. R. Kmetz and F. K. von Willisen, Plenum Press, NY, 1976. T. P. Brody.

"Real-time Video Performance of TFT-Addressed EL Panels" IEEE/SID Biennial Display Conf., New York, Oct. 1976. T. P. Brody, F. C. Luo, Z. P. Szepesi, D. H. Davies, P. G. Kennedy.

"A 350 Character TFT-EL Display" Presented at the 1975 International Electron Devices Meeting, Washington DC. Published in p. 250 of the Proc. IEDM, 1975. T. P. Brody, F. C. Luo, D.H. Davies and Z. P. Szepesi.

"Large Area Masking Techniques for TFT Arrays", SPIE Seminar in "Developments in Semiconductor Microlithography" San Jose CA April 1977, T. P. Brody.

"Modern Trends in Display Technology" IEEE Device Res. Conf., U. of Utah June 1976, T. P. Brody.

"Performance Characteristics of Thin-Film Transistors Used in Large-Area Integrated Solid-State Displays, E. W. Greeneich and F. C. Luo, Proc. 24 IEEE-ECC Conf Washington DC 1974 p 16

In addition eleven quarterly reports were published on this contract.

APPENDIX I

DESIGN OF AN EL-PANEL DISPLAY EXERCISER

In order to subjectively assess the performance of completed panels, it is essential to operate the panel in a manner approaching its eventual utilization. The thin-film TFT integrated matrix panel is so novel, however, this was not an easy task. It was decided that a suitable system for initial demonstration should present alphanumeric data, refreshed at rates approaching those of TV video systems. As explained above the multiplexing matrix approach to displays, whether they be TFT, gas discharge or whatever, usually requires a line at a time addressing mode, i.e., although each element is individually addressed the display information is presented with a line by line refresh mode. In the exercised panel alphanumeric characters are displayed in a 5 x 7 element format, i.e., one character in each 5 x 7 rectangle. This same character was repeated several times in one direction with a 2 element gap between each unit display cell. Seven separate characters were available laterally along the panel and then repeated. In later versions this unit character block was increased to 14. The entire display is refreshed once every 1.2 milliseconds on a one row at a time basis at 60 Hz. 120 Hz and 30 Hz was also available. The 100 μsec for loading column drivers and the remaining 60 μsec for transferring voltage to the storage capacitors. Individual intensity control for each alphanumeric cell was not

available, but overall intensity variability for the whole display was adjustable through change in the amplitude of the EL-power supply. The exerciser was designed to be fully portable and self contained and supplies both the high frequency power to the EL as well as the appropriate gating signals.

A logic block diagram is shown in Fig (46).

A description of operation of the logic and power supply design etc is available in the quarterly reports.

Several complete exercisers were constructed. A view of the equipment, with blank panel attached, is shown in Fig (47). As illustrated the whole unit is packaged in a conventional suitcase and is readily portable. To provide a quick check on the logic functions a simple 5 x 7 element LED display was made and interfaced with the exerciser.

In the later versions the heavy commercial power supplies were replaced by solid state supplies of our own design. This improved the possibility and allowed the entire units to be packaged in one suitcase.

All the exercisers functioned to their design requirements and on the whole were reliable and rugged.

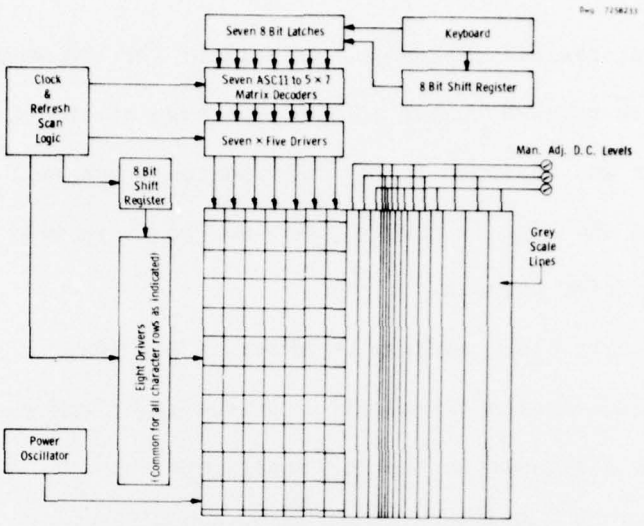

Fig (46) Logic block diagram of exerciser

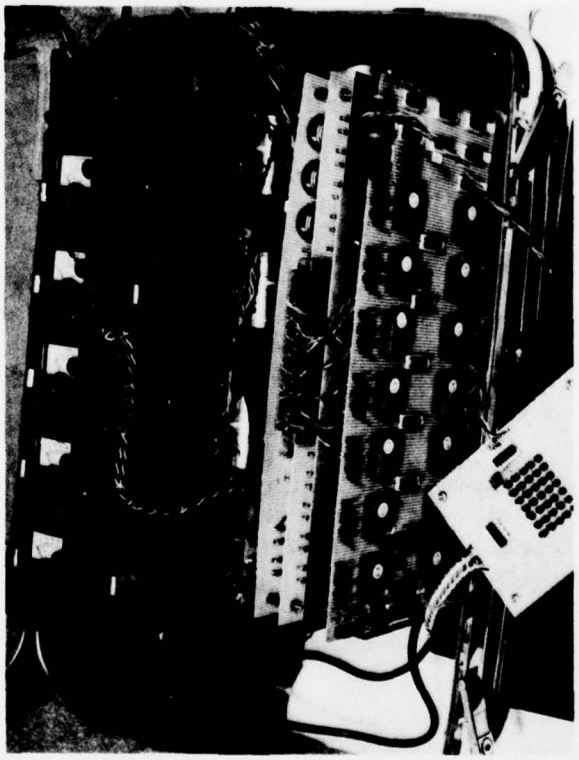

Fig (47) A view of the exerciser

APPENDIX II

LIVE TV ON THE TFT-EL DISPLAY

We have reported above on 6 x 6 inch, 20 and 30 lines/inch electroluminescent displays, controlled by a matrix-addressed array of thin film transistors deposited directly on the panel. These panels were of course designed for alphanumeric data display, i.e., simple ON/OFF operation of the display elements.

However, since the thin film transistors controlling the brightness of the individual display elements are capable of analog operation, we attempted to operate the panels with video inputs.

To this end, an exerciser which was originally designed to place video imagery on our 6 x 6 inch liquid crystal display, was adapted to provide the higher voltages required to drive the EL panels.

A 3-bit grey scale representation of a TV line is stored in a shift register, and applied to the panel through D/A converters at a line at a time. In operation, during the odd frame period TV line 1 is stored and, during line period 3, is entered into panel line 1. TV line 5 is entered into panel line 2 and so on. In the even frame period, TV line 2 is stored and entered into panel line 1 during line period 4, then TV line 6 is stored and entered into panel line 2, etc.

The experiment was entirely successful, and good quality moving television imagery, taken directly from off-the-air signals, could be displayed on all our alphanumeric screens. Particularly satisfactory is the complete absence of smear from fast-moving images.

Panels with both green or white EL phosphors have been successfully operated. Highlight brightnesses over 30 fl, and good visibility in normally lit rooms have been obtained, consistent with low overall power consumption. With typical imagery at good room light legibility the panels dissipated about 2W. The panel response was sufficiently uniform so that the quantization contours (caused by the 3-bit grey scale input) could be clearly seen across the image.

Substantially better performance is expected from panels designed specifically for television displays. However, the results so far provide a strong feasibility proof of the high potential of TFT-matrix addressed displays for video applications. Fig (48) and Fig (49) illustrates the results. It should be noted that this effort was not directly supported by USAECOM but was a company funded effort.

Fig (48) TV operation on the 6" x 6" 30 lpi display

Fig (49) Dr. F. C. Luo holding the TV display

APPENDIX III

ANTICIPATED FUTURE DEVELOPMENTS

This program has been a convincing demonstration of the validity of the basic concept of active, thin film matrix addressing for solid state display. Further the original premise that use of the active matrix allows selection of an optimal media by removal of the constraints imposed on the media by passive networks is proven. Hence the remarkably good power efficiency of powder ac-EL phosphor is able to be utilized despite the absence of a usable threshold in this display medium. The result is an active (light emissive) display having reasonable brightness, excellent low power needs, fast enough response to real time TV, grey level rendition and hence suitable for multifunctional use (alphanumeric, graphics and imagery). Resolution is reasonable (∿30 lpi) and the percent lit area per cell can be up to 100%.

Having achieved this goal it is reasonable to ask what's next? The following briefly states the directions that the program is taking as of the date of this report.

(1) Improved Performance

Work is underway to increase the resolution level; circuits at 128 and 70 lpi have been made although with smaller areas. An attempt is also being made at a small full TV line (500) 1" x 1" TV display. To improve the optical properties, of the display, in

particular the legibility is bright ambient light, the powder ac-EL phosphor is being replaced with the newly "rediscovered" thin film ac-EL. The TF-EL phosphor as optimized in recent work at these laboratories is compatible with the TFT device parameters developed in this program. The transparent phosphors allows the use of black underlayers with consequent contrast enhancement in high ambient light levels.

A further objective is the achievement of a "perfect" display, i.e. one with no defects. The residual sources of defects are believed to be tractable deriving as they do from substrate and mask contamination. Improvement in environment cleanliness (to class 100) and physically integrating the glass/mask cleaning process with the deposition process so that minimum exposure and handling occurs is being implemented. A further more important development is the potential offered by automated wafer probe test equipment. Recent results indicate that such equipment can scan and test an entire display circuit in reasonable times. Further the test results can be printed in map form to allow instant interpretation and the first real potential for circuit repair. The prober itself can be easily modified to incorporate circuit short elimination and possibly open patching.

With these factors, now in development, the achievement of perfect, defect free, displays is not only possible but ought to be likely with reasonable yields in production.

(2) Added Features

The next obvious extension of the technology is the development of an integrated display i.e. to provide the "input" decoding to the X and Y matrices, and possibly the timing and sequencing functions as part of the panel. This is of course possible with the versatility of TFT technology, a viable thin film shift register suitable for driving the 6" x 3" display has been developed and demonstrated.

A further development is the nonvolatile "memory" TFT and the incorporation of the device into the matrix. Such a device provides elemental storage and hence eliminates the need for an elemental capacitor and the logic device. The simpler structures offer the opportunity for higher resolution devices.

(3) Manufacturing Potential

As a result of detailed analysis an alternate TF circuit process concept was considered as more appropriate for manufacturing methods. The inevitable build-up on the mask sets, the lack of pattern registration possible with X-Y methods and the time needed to reset X-Y location numbers all make this approach less attractive for production. The use of "dedicated pattern" masks has been investigated with a completely computer controlled deposition facility; good quality displays have been made on this equipment. For further information see the Quarterly Reports on Contract DAAB07-76-C-0027.

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